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A Novel Design of High-Throughout Hard Ware Implementation for Video Decoding based on H.264

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Abstract
In this paper, a novel high-throughput implementation for video decoding based on H.264 is proposed to improve the decoding efficiency. H.264 provides many new functions than previous video coding algorithm that bring more complex computations, Therefore, How t implementation of the decoder efficiency becomes a challenging. Research shows in the decoding flow there are many data dependency among different symbols. Especially in the entropy decoding this dependence is most obvious. Thence the CAVLC decoder requires large computation

time, which administrates the overall decoder system performance. In order to improve performance of CAVLC decoder, the CAVLC decoder procedure is first analyzed. This paper presents a one decoding procedure double level resolve design for H.264 CAVLC decoding. In the proposed design, we exploit a predict method to achieve double level decoding. Besides the implementation of heading one detector is based on statistical results to improve efficiency of the decoder. Emulation results show that the calculation operation period of the implementation architecture can be reduced about 28% compare with the tradition CAVLC architecture. The maximum frequency can be larger than 216 MHz.
Key words: H.264, ENTROPY DECODING, DOUBLE-LEVEL, PREDICTION MECHANISM.

1. Introduction

In recent years, with the rapid development of multimedia technologies, multimedia systems have become essential. There are several efficiency video coding standards that have been proposed to compress multimedia information while ensuring the quality of the video. H.264 is one of these video coding standards. H.264 adopted the advanced coding algorithm and provides enhanced coding efficiency for a wide range of applications (ITU-T Recommendation and International Standard, 2009), H.264 provide further improvements of video data compression ratio to preserve excellent quality when comparing to previous video standard. It is currently one of the most powerful video standards. In previous research the complexity profiling of H.264 decoder have been discussions in depth (Quan, X.,et al, 2005).The result shows in Fig.1, the computational complexity of context-based adaptive variable length decoding (CAVLD) is about 28 percentage of total H.264 decoder computational operation. The computational complexity of MC in H.264 decoder is about 35 percentages. It can be easily improved by using the parallel processing method. For different video coding standards, variable length coding (VLC) is a widely used coding technique. CAVLC is a variable length decoding method adopted in H.264. This decoding method has strong data dependency between the consecutive parameter make it hard to exploit the pipeline and parallel architecture in hardware implementation. Therefore, CAVLC decoding is usually the bottleneck of H.264 decoder. Thus, propose an efficient CAVLC decoder hardware is of practical importance. Researchers pay much effort in how to design a decoder with lower calculating cycle and more efficiently (Moon, Y.H, 2007; Chang, C.H. et al, 2007). Biswas cut off the critical path to improve throughput by restricting the bits of process to 16 bits (Biswas, M.A.J., 2006). Yu decoded two runs with parallel processing in the same cycle (Yu, G.S., et al, 2006). Wen used six decoders to decode all runs in three cycles, but this kind of architecture induces a large delay on critical path (Wen, Y.N., et al, 2006).

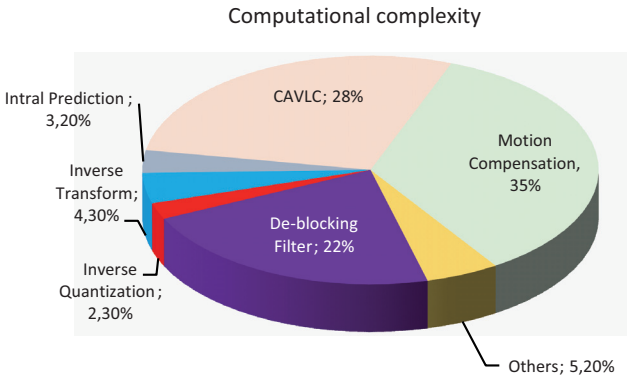


Figure 1. The Complexity Profiling of H.264 Decoder

However, since the length of different code word is variable, the boundary between consecutive code word cannot be determined until the previous code word is decoded, which limits decoding efficiently. So the pipeline and parallel architecture are not suitable in traditional implementations. Apart from this, entropy decoding the variable-length codes are normally based some tables which are defined in advance.

In this paper, after a depth analysis of the CAVLC coding algorithm (Di, W., et al, 2003), we propose a novel implementation for H.264 video decoding. Two novel method been proposed to improve the efficiency of the decoder which are double level decoding and heading one decoder based on statistics result. This paper is organized as follows. At first, this paper introduces the decoding flow of H.264 decoder and a depth discussion entropy decoder in H.264 decoder in section II. The proposed double-level CAVLC decoding design and the heading one decoder based on statistics result are illustrated in Section III. The Implementation performance is shows in Section IV. Finally, we conclude this paper in Section V.

2. H.264 Decoder Process Flow

H.264 video compression standard has high data compression rate therefore need a large amounts of calculation operation during the decoding process (Wiegand, T., et al, 2003).The flow diagram of H.264 is shown in Fig.2. The flow diagram shows that entropy decoder decomposition the coded video bit

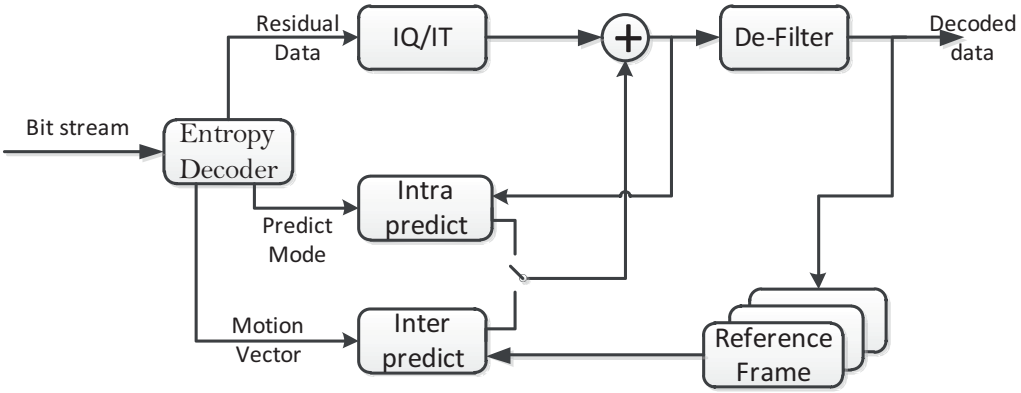


Figure 2. The Decoding Diagram of H.264

stream in to code word, such as the transformed residual data for Inverse Trans/Inverse Quant (IT/IQ), motion vectors for Inter Prediction (Chen, Z.Y., et al, 2013) and predictive modes for Intra Prediction (Jiang, W., et al, 2012). Similar to previous video coding standards, H.264/AVC adopts transform coding of the prediction residual. However, in H.264/AVC, the transformation is applied to 4×4 blocks, which is an integer orthogonal approximation of traditional Discrete Cosine Transform (DCT). A quantization parameter is used for determining the quantization of transform coefficients in H.264/AVC. According to this quantization parameter, as well as the position of each coefficient inside the macro block, a Level Scale variable is derived to inverse quantize these coefficients. The intra prediction utilizes spatial correlations of neighboring blocks, and the inter prediction utilizes temporal correlations of neighboring frames. At any one time, only one prediction mode, intra or inter, is activated. The prediction results are summed with residual blocks to derive reconstructed blocks. De-blocking filter is required to reduce these annoying blocking artifacts.

In the forehead discussing, we describe the entropy decoding is usually the bottleneck of H.264 decoder. Hence we specially focus on entropy decoding procedure. In H.264 video compression standard, during the coding procedure the quantized residuals of each 4 × 4 block and each 2 × 2 block are encoded in zigzag scan order by an entropy coder. So during the decoding procedure must take an entropy decoding operation at first. Fig. 3 shows the typical steps of CAVLC decoding algorithm. There are five steps to encoded one code word. Hence a typical CAVLC decoding algorithm can be divided into five steps. These syntax elements are defined as follows.

A Coeff-Token: Trailing ones (T1) indicate the total number of coefficients with absolute value equal

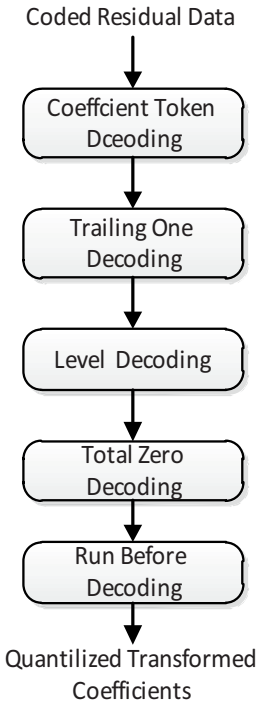


Figure 3. The Flow of CAVLC

to 1. The first VLC, named Coeff-Token, encodes both the number of total non-zero coefficients and the number of total T1.

B Sign of Trailing Ones: For each T1 decoded, its relevant sign flag is derived from a single bit, starting from the last T1.

C Level: The levels (sign and magnitude) of the remaining non-zero coefficients are encoded in reverse zigzag order, starting from the highest frequency coefficient and running backwards to the DC coefficient. Each level has two parts, a prefix and a suffix which will be decoded separately. With the end of each level decoded, the length of suffix might change based on the current level been decoded.

D Total-Zeros: The sum of all zeros preceding the last non-zero coefficient is coded with the total zeros LUT. The LUT entry is determined by current

input bit stream and previously decoded Total Coeff, representing the context adaptive feature of CAVLC.

E Run-Before: In the last step, the number of zeros preceding each non-zero coefficient (run before) is decoded in reverse zigzag order, starting from the highest frequency coefficient and working backwards to the DC coefficient.

An example for typical CAVLC decoder which takes one cycle for one symbol is shown in Tab.1 and Fig.4.

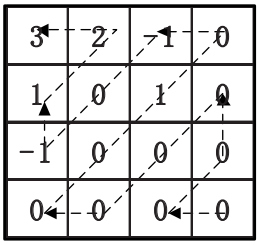


Figure 4. Reverse Scan Magnitude and Their Transmitted Bit Stream

Table 1. Decoding Procedure for Example

Input Bitstream: 0000100_01110100_01011101_0			
Symbol	Code word	value	Output array
Coeff_token	00000100	Tc=6,T1=3	N/A
Sign of T1	0	+	1
Sign of T1	1	-	-1,1
Sign of T1	1	-	-1,-1,1
Level	1	+1	1,-1,-1,1
Level	010	+2	2,1,-1,-1,1
Level	0010	+3	3,2,1-1,-1,1
Total zeros	111	2	3,2,1-1,-1,1
Run before	01	Zeros left=2;run=1	3,2,1-1,-1,0,1
Run before	0	Zeros left=1;run=1	3,2,1-1, 0,-1, 0 ,1

3. Algorithm Optimization and Hardware Implementation

From the above discuss, the main obstacle is the level decoding procedure. which needs large calculation operation. In addition, CAVLC implementations can not directly use parallel processing mechanism to improve the decoding efficiency. Since the boundary between successive code-words are indistinguishable that lead to an unavoidably long critical path. Thus, both parallel decoding and pipeline scheme can not be used for the level decoder. A effective solution needs to break the inter level dependency. Hence, in the followings, we will first analysis the characteristics of the level decoding flow, and then propose two effective proposal.

3.1. Double level decoding scheme

Fig.5 shows the flow diagram of the level decoding. There two parts: bit stream scanning process and level computation in the level decoding procedure. Each level bit string is constituted by level-prefix and level-suffix. The level prefix is a series of "0" bits and ending with a "1". Hence, need a heading one decoder to the decoding Level prefix. The resolve Level suffix, which indicate the length of the level suffix. After the suffix parameter of the level decoding is completed, the length of the suffix can be calculated.

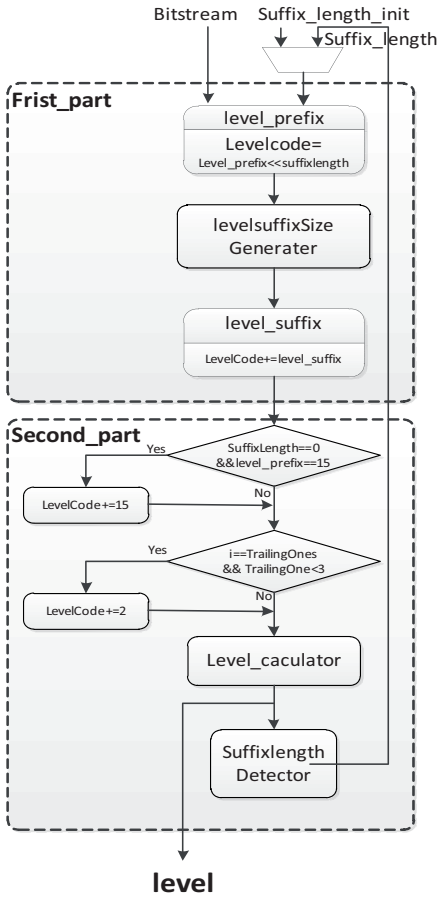


Figure 5. The Flow Diagram of The Level Decoding

From the prefix value and suffix value the level code can be calculated as the following formula:

$$\text{Level bit stream} = [\text{prefix}][1][\text{suffix}] = [0.....0]\,[1][\text{suffix}] \quad (1)$$

$$\text{Level Code} = (\text{Level Prefix} << \text{Suffix Length}) + \text{Level Sufix} \quad (2)$$

$$\text{Level} = (\text{Level Code} + 2)/2 \quad \text{Level Code is even} \quad (3)$$

$$\text{Level} = (-\text{Level Code} - 1)/2 \quad \text{Level Code is odd} \quad (4)$$

$$\text{Code Length} = \text{level\_prefix} + 1 + \text{level\_suffix} \quad (5)$$

After the level code is get, the level can be calculated from the level code. At first needs to make some adjustments of the level code according to some special conditions. When the level code is odd, the adjustments formula is level=(-Level_Code-1)/2 . On the contrary, When the level code is even, the adjustments formula is Level= (Level_Code+2)/2.After the level is get, enter the next suffix length adjustment procedure. The reason of adjustment is when the absolute value of level tends to be large the suffix length also tends to be long bits. So the suffix length of the next level needs some enhancement.

From the above the main obstacle of parallel scheme level decoder is the unknown boundary between two successive levels.

In a typical implementation of the entropy decoding, only the last procedure of previous level decoder can we get the suffix length of the next level. To break the data dependency and improve the decoding efficiency of the entropy decoder, Heng,YL.. proposed a modified suffix length detector (MSD) approach((Heng, Y.L., et al, 2008)). Fig. 6 show the MSD modified decoding diagram which can calculate the next suffix length in advanced. The MSD input is level prefix value. So once the level prefix decoded we can calculate the code word length of the next level.

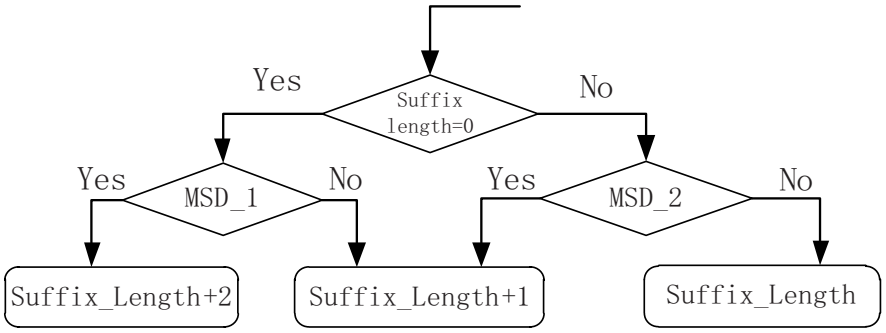
To further improve the decoding efficiency of the entropy decoder and make full use the advantages of MSD decoder, proposed a double-Level decoder based on a predict mechanic. Because there is certain correlation between the value of the current and the next suffix length. In general, if the value of the current level is less than a threshold the suffix length of the next level keep the same as suffix length of current level. Otherwise plus one bit based on suffix _length of current level or take some special adjustment. Therefore propose a prediction mechanic which contains two predict module simulate the suffix length for the next level. Achieved double level value decoding structure and improve the efficiency of the entropy decoder.

Fig.7 shows the flow diagram of proposed based on prediction mechanic double Level decoder implementation. In the propose flow diagram, first introduced MSD structure into the prediction module. The introduction of MSD structure will reduce the entropy decoder critical path length. It is possible to achieve effective prediction.

3.2. A novel design of heading one detector based on statistic

Besides the suffix resolve in the entropy heading one detector is a heavy use operating. For in-depth analysis of heading one detector operation in the entropy decoder processing. Carry a statistics of the heading one detector result.The result shows as the follow Tab 2.

Seen from the Table of the heading one value average of the two mode intra and inter prediction of statistical laws have slight difference.However, the overall trend is the same: The probability of a large front, in the back of a small probability. Aware of the statistical regularities in the table,propose a priority implementation of heading one detector based



MSD_1: (first_level&&TrailingOnes<3&&level_prefix>3)||(level_prefix>5)
MSD_2:(first_level&&TrailingOnes<3&&suffix_length=1&& level_prefix>1)
||(level_prefix>2)

Figure 6. MSD

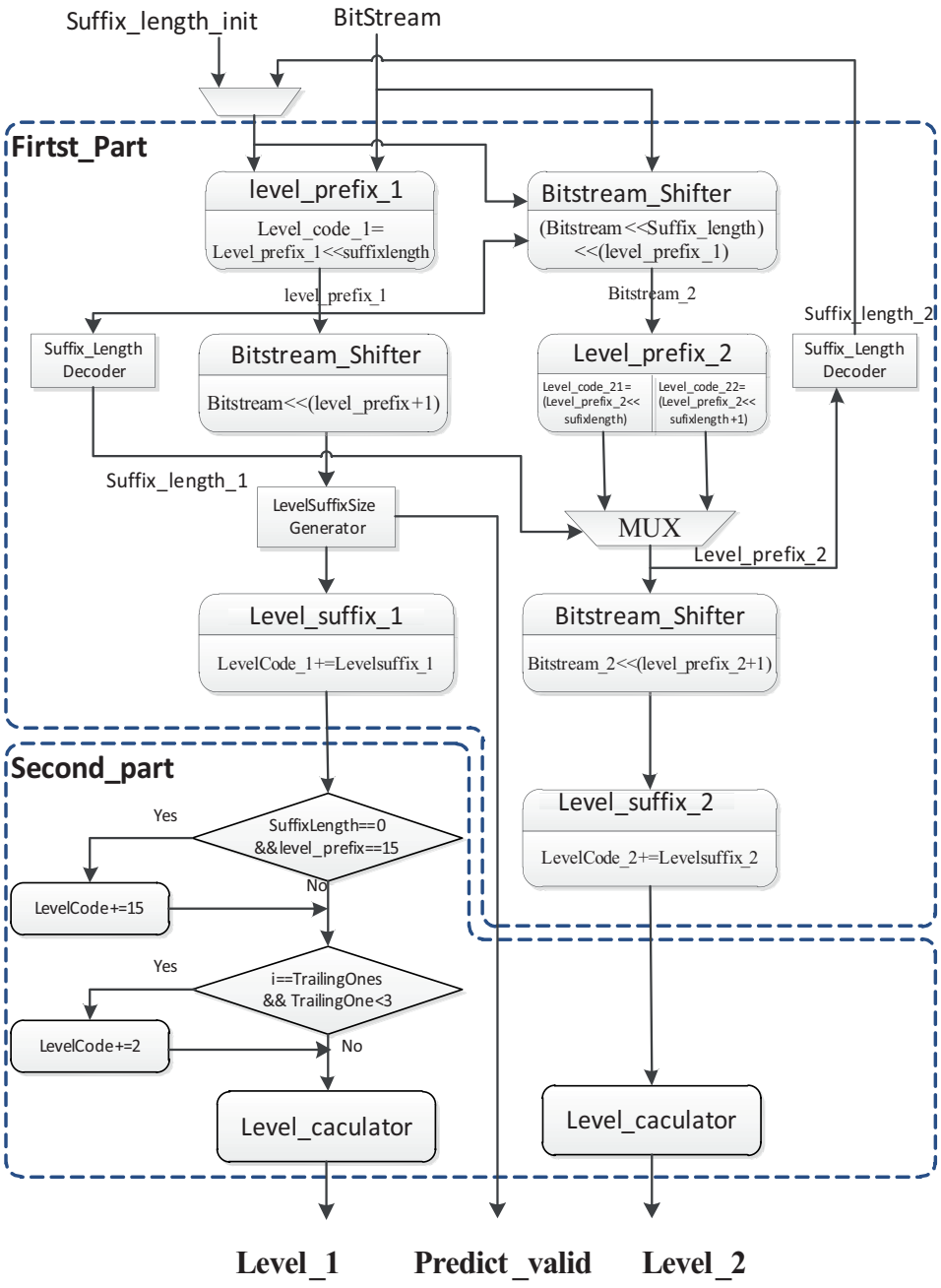


Figure 7. The Proposed A Double-Level Decoder

Table 2. Statistic Result of Heading One Position

Statistic result of heading one position			
Position	Whole bit stream	Intral frame	Inter frame
0	55.36%	51.37%	56.61%
1	24.15	24.36%	24.08%
2	11.16%	10.70%	11.31%
3	5.49%	6.21%	5.26%
4	2.17%	3.69%	1.72%
5	0.88%	1.6%	0.65%
6	0.41%	0.91%	0.25%
More than 6	Less than 1%	Less than 1%	Less than 1%
Average	0.8	1.1	0.7

on the Statistic result. In this implementation, the data in front of a higher priority. Realization shows as below

In this design, using a decode enable signal to control the input bit stream from bit stream buffer ,shows as Fig.8. If enable is set , represent read 16 bits data from the bit stream buffer to the heading one decoder, else the heading one detector is suspend to reduce unnecessary power consumption. The entire detector is consists of three parts. Dec2, which has the highest priority to detect the bit 0 and bit 1 whether there is a “1”. If a “1” is found in dec2, outputs the corresponding position of the heading one . The location information is passed to the final priority encoder to generate a heading one position. Meanwhile, the lower-priority Dec4 and lowest priority Dec10 be disabled to save power. On the contrary, there is a 20% possibility that the Dec2 will not find a "1" and Dec4 thereafter enabled. More rarely, both Dec2 and dec4 not gives results, and then DEC10 will be activated, but only 1% possibility. Dec2, Dec4 and Dec10 is selectively output by the priority to detect the heading one position of whole 16bit input. So a lot of power is saved because priority-based heading one detect.

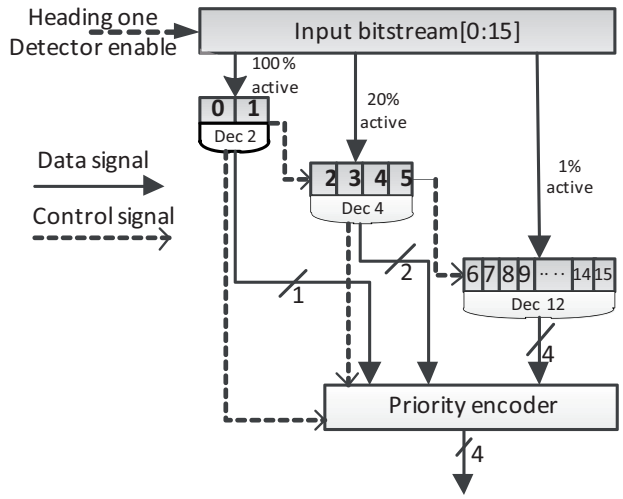


Figure 8. The Priority-Based Heading One Detect

4. Implementation Results

The entire decoder is described in Verilog-HDL code. The FPGA-oriented RTL code was synthesized, translated, placed and routed by Xilinx ISE, and simulated by ModelSim. FPGA verification is carried out on Xilinx Virtex5 emulation board after software function simulation. The 300frames QCIF video sequences are used for testing. They are encoded by JM software. In Fig.9 the QCIF Akiyo@300 frames bit streams is decoded using the proposed decoder.The decode result show as follow:

Figure 9. The Output of Decoder

4.1. Performance Evaluation and Comparison

By making use of suffix length predict strategy based MSD and the statistic result of heading one detector. the data throughput and power consumption of CAVLC decoder improved obviously. Compared with conventional implementation of single level decoder, the simulation result shows that the proposed architecture is high decoding efficiency. Performance evaluation of the decoder are summarized in Tab.3.

Table 3. Simulation Result

	Foreman	Akiyo	Parkrun
Single level Decoder(cycle)	1146031	1679432	1512467
Proposed double level decoder(cycle)	896038	1282009	1200371
Reduced percentage	28%	31%	26%

The Tab.3 shows the clock resource consumption comparison between different designs to decoding the same video bit stream. The result shows he proposed double level entropy decoder deduce 28.3% clock cycles consume than the conventional architecture on average . The maximum operating frequency of the processor is up to 216MHz

4.2. Hardware implementation and resource consumption

We use Verilog HDL to implement the proposed design and ISE for synthesis. The synthesis report shows that the maximum operation frequency can achieve to 216 MHz. the cost numbers of LUT is 26,586 and the cost number of slice register is6,479 and the data throughput is 960K.While the Akiyo@300 frames bit streams is 640K.So this implementation can achieve real-time decoding. Tab.4 shows the result of synthesis.

Table 4. Synthesis Result

Number of Slice Registers	6,479
Number of Slice LUTs	26,586
Max frequency	216Mhz
Dynamic power	157.01(mW)
Throughput	960K

5. Conclusion

In this paper, a double level CAVLC decoding architecture and priority-based heading one detect is posed which is designed to promote the data throughput and reduce the power consumption. By analyzing the CAVLC algorithm and suffix length update discipline propose a next suffix length predict strategy. With an aid of the predict strategy, the proposed architecture can break the data dependency. So we can use the parallel structure to design a entropy decoder to promote the decoding speed of the conventional decoding procedure suggested in the H.264 standard. In the best case, double level decoder can calculate two levels at once. Thus, high throughput can be achieved. Besides, a novel priority-based heading one detector for CAVLC decoding of H.264 is propose. It exploits the statistical result of detecting output and a partition the input bit stream in to three part of the heading one decoding detector. Compared with a conventional design of entropy decoder, the power consumption of the proposed implementation can be reduced by more than 2 times while decoder logic operation output remains unchanged. The proposed implementation has successfully been verified by FPGA development board to verify that the decoder logic functions of the proposed H.264 decoder.

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Community Discovery Optimization Algorithm in Social Network

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Abstract
As for the present community discovery and compression algorithm ignoring the issue of network community structures, this paper proposes a community discovery GS algorithm and community compression SNC algorithm. On the basis of proposing the theorems and corollaries related to the importance of the nodes in community discovered by topological method. GS algorithm discoveries the important nodes on different levels in community, and then through social networks compresses SNC algorithm and according the importance of the node compresses the community. Experimental results show that: the proposed algorithm can maintain the relationship between the communities during the compression process. It has a good community compression, in which the ratio can up to 0.95, and at the same time it can retain the important nodes in the community or community basic structures.
Keywords: FIGURE COMPRESSION, COMMUNITY CISCOVERY, ROUTING SELECTION, NODE