Super-Threshold Adiabatic FinFET SRAM with PAL-2N Logic

Yuejie Zhang, Jianping Hu, Tianfang Ma, Beibei Qi

Faculty of Information Science and Technology, Ningbo University, Ningbo 315211, China

Corresponding author is Jianping Hu

Abstract

With IC process scaling, the leakage consumption has been an important factor in the power consumption of IC chips, which limits the scaling of SRAM. The FinFET device has the advantage in lower leakage current and higher on-state current than the CMOS devices. In this paper, a FinFET SRAM is verified by using adiabatic computing. All the circuits of the SRAM except for the storage array are realized by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) circuits. The storage uses 8T cell that can improve the read margin and keep the write current against the synchronous read/write disturb. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The results indicated that the energy consumption of the adiabatic FinFET SRAM decreased 49% compared with the SRAM based on CMOS devices.
Keywords: SUPER-THRESHOLD, SRAM, ADIABATIC, FINFET, LOW POWER

1. Introduction

The power consumption has been a critical concern in the VLSI circuit design. Especially the power consumption of embedded SRAM is a significant concern in processors [1]. The SRAM circuits have large storage density and small access latency, and thus it is used extensively in processors as on-chip memories [1]. Recently, there are more and more low-power SRAMs that were reported.

The energy consumption is composed of two components: dynamic consumption and static consumption [2]. The dynamic energy consumption can be reduced by many methods, such as adiabatic circuits, sub-threshold, multi-threshold, and low voltage technologies [3-5]. The total energy consumption of a circuit per cycle are expressed as

$$E_{total} = C_L V_{DD}{}^2 + V_{DD} I_{leakage} T \qquad (1)$$

where C_L is load capacitance of the inverter, V_{DD} is source voltage of the inverter, $I_{leakage}$ is average leak-age current from supply to the ground, and T is operating cycle of the circuits.

The adiabatic circuits have advantages compared with the conventional CMOS circuits in low power aspects [5]. The conventional CMOS circuits will consume a portion of energy in the form of heat dissipation. The adiabatic circuit uses the AC power supply instead the DC power supply of the conventional CMOS circuit. In a period of AC power supply, half of the energy consumption is stored in the node capacitance. The energy consumption stored in the node capacitance can recover to the supply voltage in adiabatic circuits. The formula of energy consumption in a cycle of the AC power supply when the adiabatic circuit completing a charge and discharge of the load capacitance is:

$$E = 2(\frac{RC_L}{T}) \times C_L V^2 \qquad (2)$$

We can conclude that the E and T are proportional to the inverse ratio. When the T is large, E becomes

small. Therefore, the adiabatic circuits can effectually reduce the dynamic consumption, which can avoid the heat dissipation in charging and discharging period. The several adiabatic SRAMs have been reported, which were as a kind of the low-power SRAMs.

When the CMOS IC technologies scaled down to 25 nm, the CMOS technologies encounter challenge such as short channel effects (SOC), which increase the leakage current and power consumption [6-9]. Among the recently reported novel devices, FinFET device shows excellent performance and low-power characteristic than the CMOS device. The FinFET transistor is the candidate replace of CMOS transistor. FinFET technology is a possible solution to achieve a better power/performance trade-off for SRAM cells.

In addition, a simple and effective way to reduce energy is to scale down the supply voltage. The dynamic energy and the leakage dissipation decreased significantly as voltage scaling down. Scaling voltage to the near-threshold region (near the threshold voltage V_{TH}) can greatly reduce the dynamic energy. The low-power SRAMs have been reported to scale the voltage of the power supply [10]. Due to the CMOS device of near-threshold circuits operates on medium weak inversion, the CMOS near-threshold circuits are only suitable for mid-performance applications. Moreover, the near-threshold circuits that work in a moderate inversion have large performance deviation [11].

To our knowledge, adiabatic SRAMs have not been explored using FinFET devices. In this paper, we target to verify FinFET SRAM circuit based on adiabatic logic in the super-threshold region. Al the circuits of the SRAM except for the storage array is realized by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) circuits. The storage uses 8T cell that can improve the read margin and keep the write current against the synchronous read/write disturb. All circuits are simulated with HSPICE using the PTM (Predictive Technology Model) 32nm FinFET technology. The simulation result shows that energy consumption losses of the PAL-2N SRAM based on FinFET transistor are greatly reduced compared with the PAL-2N SRAM based on CMOS device.

2. Energy Consumption and Delay

The FinFET transistor has a non-planar gate, as shown in Fig. 1. The non-planar gate rounds the source/drain structure for better controlling for the channel. The structure of the FinFET transistor can reduce the short channel effect and has a better sub-threshold rate than the CMOS transistors. In this

work, only SG (short-gate) mode is considered. The effective gate width of a SG FinFET transistor is

$$W = 2 \times n \times H_{fin} \qquad (3)$$

where n is fin number of FinFET transistors and H_{fin} is its fin height. The wider transistors are gained through multiple fins.
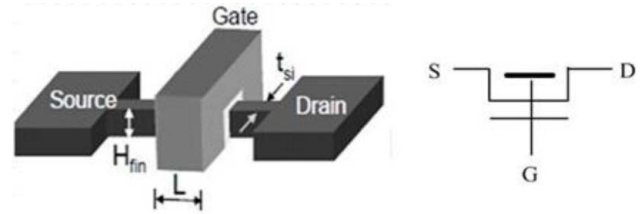

Figure 1. The structure of the FinFET transistor

Assuming that P-type and N-type FinFETs is symmetrical, when the source voltage is larger than V_{th}, the delay of a FinFET inverter can be roughly represented as

$$t_d = \frac{KC_L V_{DD}}{(V_{DD} - V_{th})^\alpha} \qquad (4)$$

where K is a parameter, and a is velocity saturation parameter. In sub-threshold regions, where the source voltage is lower than V_{th}, the delay of an inverter can be roughly written as

$$\frac{KC_L V_{DD}}{_{o\ g} \exp\left(\dfrac{V_{DD}\ V_{th\ g}}{nV}\right)} \qquad (5)$$

where V_T is thermal voltage, n is sub-threshold slope factor, and $I_{o,g}$ and $V_{th,g}$ are experiment parameter, respectively.

The EDP (Energy Delay Product) provides a comprehensive performance between delay and energy dissipation of the circuits. Fig. 2 is the EDP comparison of the CMOS device and Fin-FET device. EDP is defined as

$$EDP = E \times t_{delay} \qquad (6)$$

Combining the above equations (1), (4), (5) and (6), EDP of an inverter is given as

$$EDP = \begin{cases} \dfrac{\left(C_L V_{DD}^2 + V_{DD} I_{leakage} T\right) KC_L V_{DD}}{(V_{DD} - V_{th})^\alpha} \\ \qquad For \quad V_{dd} > V_{th} \\ \dfrac{\left(C_L V_{DD}^2 + V_{DD} I_{leakage} T\right) KC_L V_{DD}}{I_{o,g} \exp\left(\dfrac{V_{DD} - V_{th,g}}{nV_T}\right)} \\ \qquad For \quad V_{dd} < V_{th} \end{cases} \qquad (7)$$

In order to get the EDP from Hspice simulation, we let the propogation delay is

$$t_{delay} = (t_{pLH} + t_{pHL})/2 \qquad (8)$$

where t_{pHL} and t_{pLH} represent output transition time from high to low level and from low to high level, respectively.

From Fig. 2, the FinFET buffer has better performance than the CMOS buffer. The FinFET buffer achieves the minimum EDP between the 6V and 0.7V supply voltages, while the EDP of the CMOS buffer is minimized at about 0.5V. Compared with 1.0V source voltage, the minimum EDPs of the buffers based on FinFET and CMOS reduce 29% and 20%, respectively. The results shown that minimum EDPs of CMOS circuits lay in near-threshed region, while FinFET circuits have minimum EDPs in super-threshold regions.

Figure 2. EDP comparison of 32nm FinFET and conventional CMOS buffer

3. PAL-2N Circuits Based on FinFET Transistors

PAL-2N circuits consist of two main parts: the logic assignment circuit and energy recovery circuit. The logic assignment circuit is composed by two NMOS logic transistors: N3 and N4. The energy recovery circuit is composed of the PMOS transistors P1 and P2. The output node energy is recovered to the CLK through the P1 or P2. The transistor N1 and N2 muzzle the output node voltage, making it not hung up. PAL-2N circuits use non-overlapping four-phase sine power clock. The design of the power clock generating circuits is very simple. The structure of the PAL-2N buffer is shown as Fig. 3.

Fig. 4 shows the simulation of the PAL-2N buffer chain and four-phase sine power clock. The four-phase sine power clock as the ideal power clock is

used in the adiabatic SRAM in this paper. Complex logic circuits can be derived simply by replacing the NMOS pass transistor trees with the corresponding logic function blocks, ash shown Fig. 5.
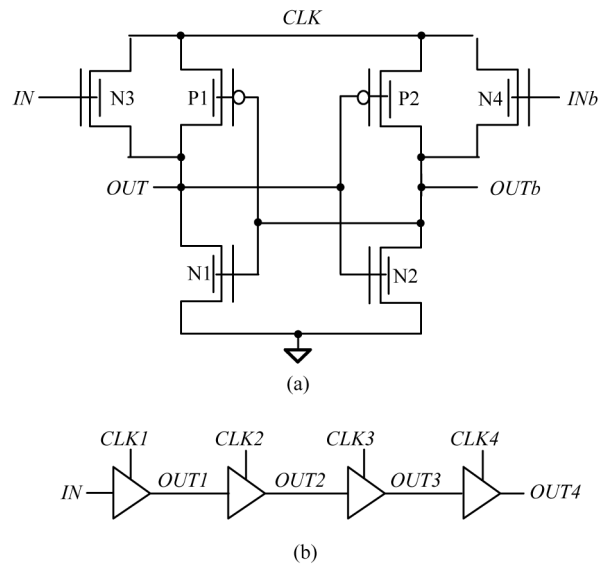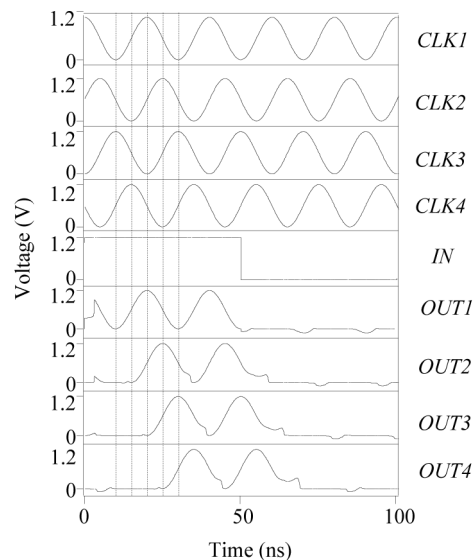
Figure 3. PAL-2N buffer (a) and buffer chain (b)

Figure 4. Simulation waveform of PAL-2N buffer

4. Design of PAL-2N SRAM

The properties of the SRAM are the functionality and density of a memory array. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins, which are determined by device sizing, the supply voltage, and, marginally, by the selection of transistor threshold voltages. In the design of PAL-2N SRAM, all circuits (the word-line decoder and the read/write driver) use the PAL-2N circuits except the storage cell matrix. The PAL-2N SRAM can reduce the overall energy consumption. The following introduces the composition of PAL-2N SRAM circuits and the storage cell in detail.
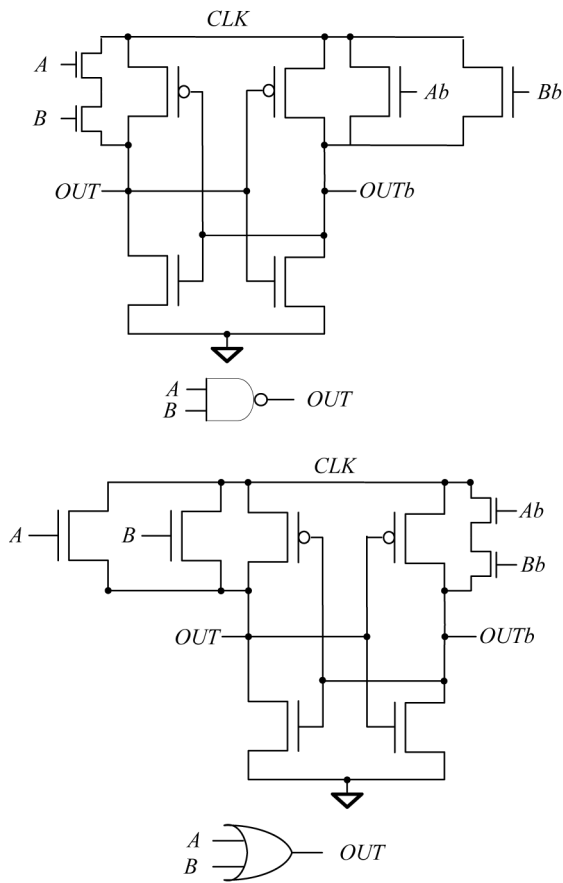
Figure 5. Basic gates of PAL-2N circuit

4.1. The Structure of the SRAM

The FinFET-based PAL-2N SRAM circuit structure is as same as the conventional CMOS SRAM structure, as shown in Fig. 6.
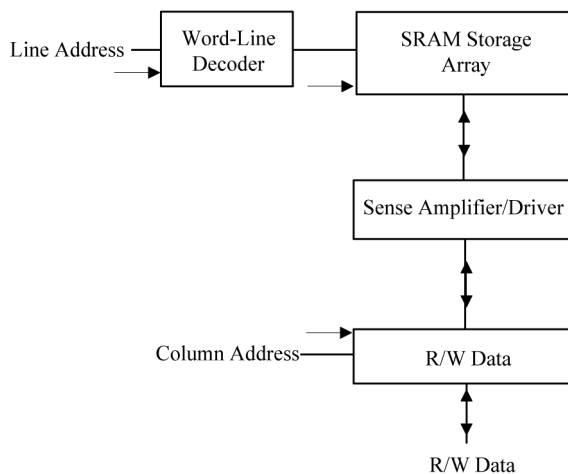

Figure 6. PAL-2N SRAM circuit structure

4.2. Storage Cell

8T storage cell is used in the design of the FinFET-based PAL-2N SRAM, as shown in Fig. 7. The cell consists of two back-to-back inverters and access transistors (N1, N2, N3, and N4). *RWL* is the read word line, and *WWL* is the write word line. The stor-age cell read data through the transistors N3 and N4. Compared with the 6T storage cell, this storage cell structure can improve the read margin, keep the write current then reduce the energy consumption, and can against the synchronous read/write disturb.
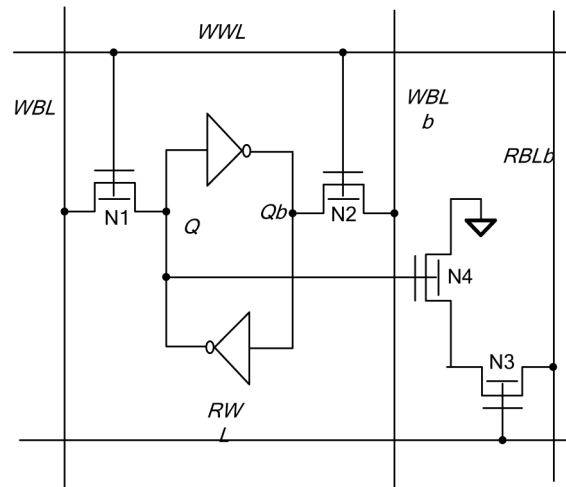

Figure 7. Storage cell

The adiabatic driver circuit is dual-rail, and the storage cell is also dual-rail. The storage cell should be designed so that a maximum signal is obtained in a minimum area.

4.3. Read/Write Driver and Sense Amplifier

The read/write driver circuit both uses the PAL-2N structure. The write driver can write the contents in the form of the PAL-2N buffer as shown in Fig. 3, which can generate WBL0…WBL31 (write bit line). The read driver circuit uses the same topology as write driver circuit. The sense amplifier circuit is shown in Fig. 8. It is composed of two back to back inverters.
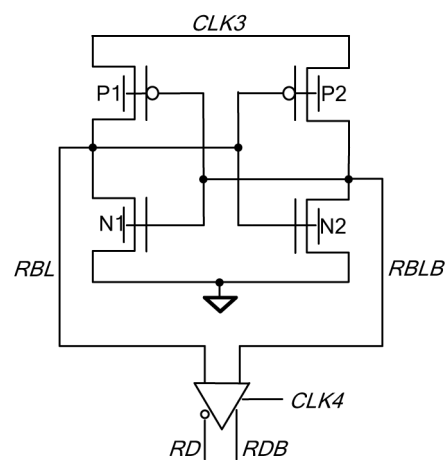

Figure 8. Sense amplifier

4.4. Word-Line Decoder

Fig. 9 shows the energy consumption of the FinFET PAL-2N word-line decoder, CMOS PAL-2N

word-line decoder, FinFET conventional word-line decoder, and CMOS conventional word-line decoder. From the simulation result, we can conclude that the FinFET-based circuits consume less energy than the CMOS circuits. Moreover, the adibatic word-Line decoder consumes less energy than the conventional one.
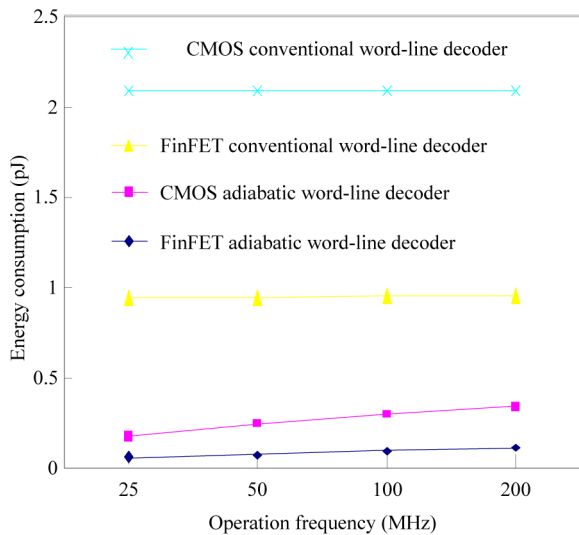

Figure 9. Energy consumption of CMOS conventional word-line decoder, FinFET conventional word-line decoder, CMOS adiabatic word-line decoder, and FinFET word-line decoder

4.5. Simulation Result of the PAL-2N SRAM

Fig. 10 is the energy consumption of the FinFET PAL-2N SRAM, CMOS PAL-2N SRAM, FinFET conventional SRAM, and CMOS conventional SRAM, from 25 to 200MHz. From Fig. 10, it is concluded that the adiabatic SRAM based on both FinFET and CMOS consumes less energy than the conventional FinFET and CMOS SRAMs.
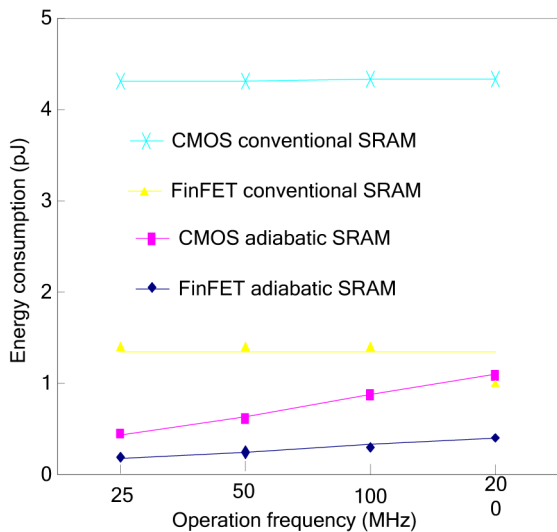

Figure. 10 Energy consumption of CMOS conventional SRAM, FinFET conventional SRAM, CMOS adiabatic SRAM, and FinFET adiabatic SRAM from 25 to 200 MHz

The adiabatic FinFET SRAM reduces 49% energy dissipations than the CMOS adiabatic SRAM at 100MHz. Table 1 is energy consumption of the storage cell, read driver circuit, and write circuit of FinFET-based adiabatic SRAM, CMOS adiabatic SRAM, FinFET-based conventional SRAM, and CMOS conventional SRAM. It is concluded that the energy consumption of the storage cell account for a small percentage. In all the four SRAMs, energy dissipations of the storage cell are almost the same. The adiabatic SRAMs reduce their total energy dissipation mostly through reducing the energy losses of logic cells such as read driver and write driver.

Table 1. Energy consumption of SRAM at 100MHz (pJ)

SRAM	Storage cell	Read driver	Write driver
FinFET-based adiabatic SRAM	0.022	0.05	0.05
CMOS adiabatic SRAM	0.022	0.18	0.18
FinFET-based conventional SRAM	0.021	0.25	0.25
CMOS conventional SRAM	0.021	0.6	0.6

The energy consumption of FinFET-based SRAM working at various voltages from 0.7V-1.0V at 100MHz is shown in Fig. 11. It is concluded that scaling down the operation voltage can effectively reduce the energy consumption. The energy consumption of the FinFET-based SRAM at 0.7V, 0.8V and 0.9V supply voltage is only 49%, 62%, and 76% of that of 1.0V supply voltage.

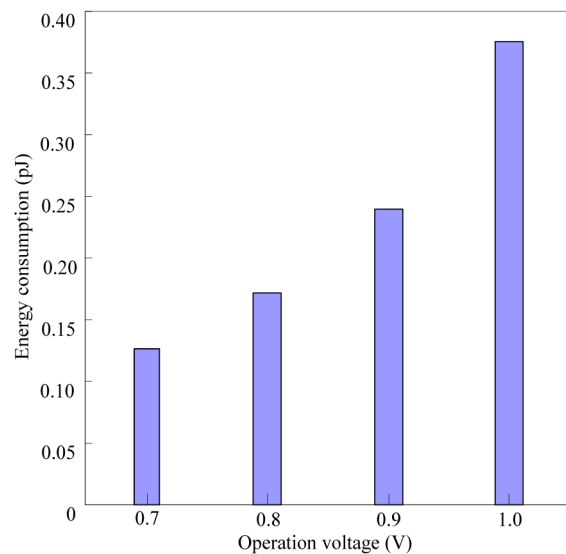Fig. 12 shows the maximum frequency of adiabatic FinFET and CMOS SRAMs at different source

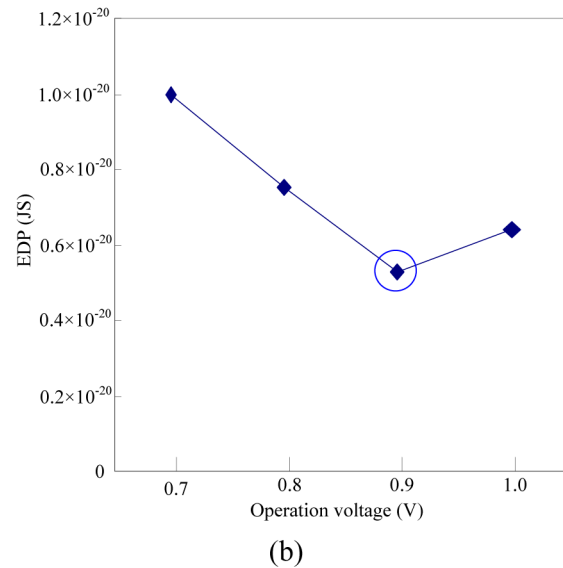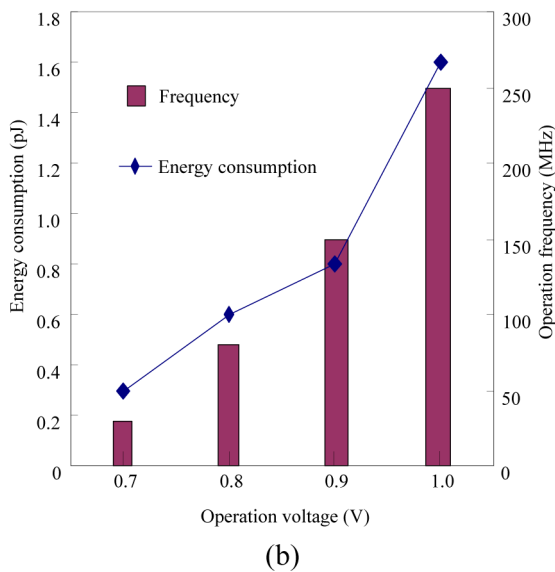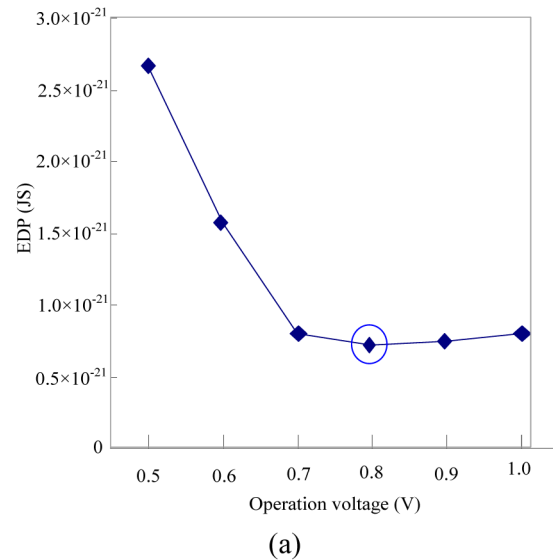**Figure 11.** Energy consumption of FinFET adiabatic SRAM from 0.7V to 1V at 1MHz

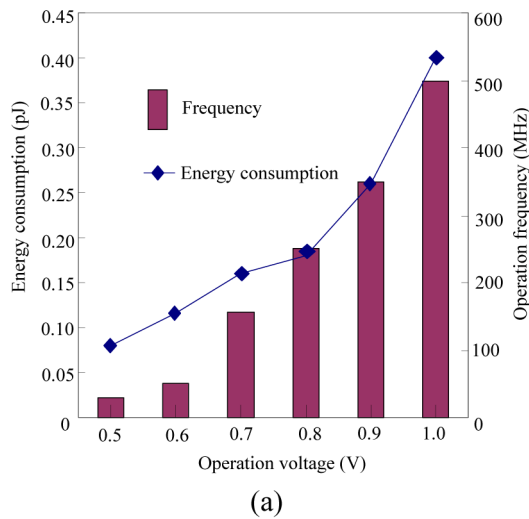(a)

(b)

Figure 12. Energy consumption per cycle at max frequency with different operation voltage. (a) Adiabatic FinFET SRAM, and (b) Adiabatic CMOS SRAM

(a)

(b)

Figure 13. (a) EDP of 32nm FinFET adiabatic SRAM, (b) EDP of 32nm adiabatic CMOS SRAM

voltages. At 0.8V source voltage, the maximum operation frequency of adiabatic FinFET and CMOS SRAMs is about 250MHz and 150MHz, respectively. The energy consumption of adiabatic FinFET and CMOS SRAMs reduces about 45% at 0.8V compared with 1.0V source voltage.

The EDP of the adiabatic FinFET-based SRAM and adiabatic CMOS SRAM is shown in Fig. 13. From Fig. 13(a) and Fig. 13(b), it is concluded that the performance of FinFET-based adiabatic SRAM is better than the adiabatic CMOS SRAM. The ranging of the operation frequency of the FinFET-based adiabatic SRAM is wider than the CMOS adiabatic SRAM. From Fig. 13(a), the operating voltage of the adiabatic FinFET SARM can be reduced to 0.5V, whereas form Fig. 13(b), the working voltage can only been reduced to 0.7V.

Conclusions

A super-threshold implementation of FinFET-based SRAM with adiabatic logic is verified in this paper. This implementation uses the PAL-2N circuits with four-phase power clock. The simulation results confirm that the FinFET-based SRAM with adiabatic logic consumes less energy than the CMOS adiabatic one. In addition, scaling down operation voltage can significantly reduce energy consumption. The FinFET SRAM operating in the super-threshold region reduces about 45% than the CMOS SRAM. The adiabatic SRAM using FinFET devices can provide better performance in low power and operating frequencies than adiabatic one using bulk CMOS devices.

Acknowledgements

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