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Super-Threshold Computing of FinFET Flip-Flops

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Abstract
Reducing the source voltage can effetely lower power dissipation of flip flops, but resulting in its performance degradation. This paper presents super-threshold computing of flip flops. The four typical flip flops, named as transmission-gate master-slave flip-flop, simplified static master-slave flip-flop, clocked CMOS master-slave flip-flop, and TSPC dynamic master-slave flip-flop operating on medium strong inversion regions are investigated in terms of settling time, propagation delay, power consumption, and power delay product. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The simulation results show that super-threshold FinFET flip flops operating on medium strong inversion regions attain about 38% power reduction with a penalty of only about 16%.
Keywords: FINFET, SUPER-THRESHOLD, FLIP-FLOP, LOW-POWER CONSUMPTION

1. Introuduction

As transistor size scales down, short channel effect of bulk MOS transistors results in very significant leakage power consumption [1, 2]. FinFETs as a 3D device have better turn-on current and lower leakage current compared with bulk MOS transistors, and

thus has become a continuation of the mainstream devices of current IC chips to replace the ordinary CMOS processes.

As portable electronic products are widely used, extending battery life has become a main goal of the IC design engineers [3, 4, 5]. Reduce the supply voltage is the most common method to reduce the power consumption of the circuits, since reducing the power supply voltage can both reduce the dynamic power consumption and also the leakage power consumption of the circuits [2]. However, reducing the source voltage would result in its performance degradation of the circuits.

In the super-threshold computing, the supply voltage of the circuits is much higher than threshold voltage of the transistors to avoid performance degradation of the circuits, but it is lower than normal standard supply voltage to reduce power dissipations of the circuits. Therefore, super threshold computing for the circuits reduces the power consumption at the expense of small performance degradation.

A flip flop is one of important cells widely used in IC chips, and its performance plays a key role for whole circuits [6-10]. In this paper, super-threshold computing of flip flops is presented. The four typical flip flops, named as transmission-gate master-slave flip-flop, simplified static master-slave flip-flop, clocked CMOS master-slave flip-flop, and TSPC dynamic master-slave flip-flop operating on medium strong inversion regions are investigated in terms of settling time, propagation delay, power consumption, and power delay product. All circuits are verified with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology [11]. The simulation results show that super-threshold FinFET flip flops operating on medium strong inversion regions attain about 38% power reduction with a penalty of only about 16%.

2. FinFET transistors

Fig. 1 shows the three-dimensional structure of FinFET [12]. The FinFET transistor is composed of a thin silicon body and gate electrodes wrapping this silicon body. The height and thickness of the thin silicon body are marked by t_{SI} and H_{fin}, respectively. The current of the FinFET transistors flow in parallel through the wafer plane. The two gates of the FinFET transistors can be shorted, named as SG (Short-Gate) mode. The two gates of the FinFET transistors can also controlled independently, which are achieved by etching away the gate at the top of the FinFET transistors to form the independent front and back gates [13,14]. The effective gate width of a FinFET transistor in SG mode is

$$W = 2 \times n \times H_{fin} + t_{SI} \approx 2 \times n \times H_{fin} \quad (1)$$

where n is the number of FinFET fins. The gate width of FinFET transistors can be only adjusted by using multiple fins.

Fig. 2 shows the simulation results of the current-voltage characteristics of 32nm n-type FinFET and conventional bulk NMOS transistors. Compared the conventional bulk NMOS, the turn-on current of the FinFET transistor is high, and thus fast operating frequency can be expected. Therefore, FinFET circuits operating on super-threshold regions have better performance than conventional bulk CMOS.

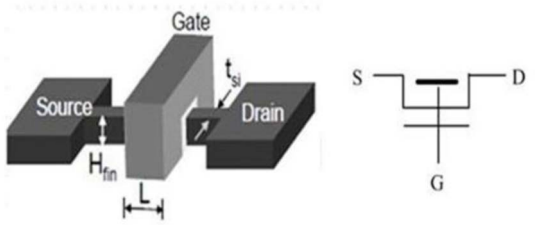

Figure 1. The structure and symbol of FinFET

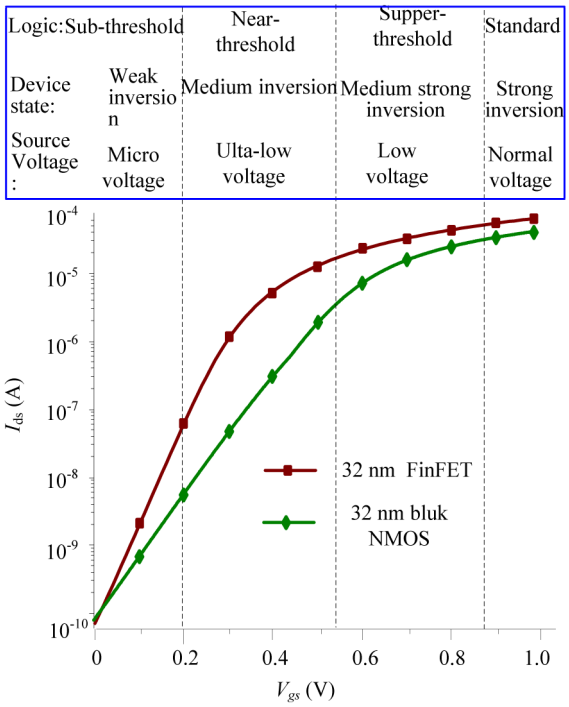

Figure 2. I -V characteristics of 32 nm n-type FinFET and conventional bulk NMOS transistor

Fig. 2 also shows that the sub-threshold slope of the FinFET transistor is larger than conventional bulk MOS transistors because of the stronger gate control on the channel. Compared with bulk MOS transistors, the leakage of the FinFET transistors is greatly reduced.

The total power consumption (P_{total}) contains the dynamic power consumption and the leakage power consumption. The dynamic power consumption and

leakage power consumption are written as, respectively

$$P_{dyn} = fC_L V_{DD}^2 \quad (2)$$

$$P_{leakage} = V_{DD} I_{leakage} \quad (3)$$

where C_L is the load capacitance, V_{DD} is source voltage, f is operation frequency of the logic gates, and $I_{leakage}$ is leakage current of FinFET transistors, respectively. Obviously, P_{dyn} and $P_{leakage}$ are reduced quadratically and linearly as supply voltage scales down.

With these two parts together, the total power consumption (P_{total}) of the FinFET logic gates are written as

$$P_{total} = P_{dyn} + P_{leakage} = fC_L V_{DD}^2 + V_{DD} I_{leakage} \quad (4)$$

When FinFET transistors operate on super-threshold regions, where the source voltage is larger than the threshold voltage of the FinFET transistors, if the symmetrical P-type and N-type FinFET transistors are employed, the delay of a FinFET inverter can be written as

$$t_d = \frac{KC_L V_{DD}}{(V_{DD} - V_{th})^{\alpha}} \quad (5)$$

where K is a delay experience parameter, V_{th} is threshold voltage of FinFET transistors, and a is velocity saturation parameter.

Between power consumption and operating speed, a comprehensive compromise is PDP (Power Delay Product), which is written as

$$PDP = P \times t_d \quad (6)$$

Combining (4), (5), and (6), PDP is given as

$$PDP = \frac{(fC_L V_{DD}^2 + V_{DD} I_{leakage}) KC_L V_{DD}}{(V_{DD} - V_{TH})^{a}} \quad (7)$$

The propagation delay of the two inverters using FinFET and bulk CMOS is compared in Fig. 3. The propagation delay is measured by

$$t_{delay} = (t_{pLH} + t_{pHL})/2 \quad (8)$$

where t_{pLH} and t_{pHL} are transition time from low (or high) level to high (or low) level. In 1.0V, 0.9V, 0.8V, 0.7V, 0.6V, and 0.5V supply source voltages, the propagation delay of the FinFET inverter is 72%, 70%, 0.64%, 56%, 45% and 38% of delay of the bulk CMOS inverter, respectively.

At 0.5V source voltage, the propagation delay of the FinFET and CMOS inverters operating in near-threshold regions is about 10 times and 4.8 times as large as 1.0V supply voltage. At 0.8V source voltage, the propagation delay of the bulk CMOS inverter operating in super-threshold regions is about 1.46 times as large as 1.0 V supply voltage, while the FinFET inverter operating in super-threshold regions has only a penalty of about 22%.

The power consumption is compared in Fig. 4. The power consumption depends highly on source voltages. It can be seen that the inverter using FinFET devices has lower power consumption than the bulk CMOS one in all power source voltages.

The power delay product of the inverters based on 32nm FinFET and conventional bulk CMOS is shown in Fig. 5. In this simulation, the period of all the input signals is defined as 1 ns. The FinFET inverter has smaller PDP than CMOS bulk. The FinFET inverter achieves the minimum PDP in the power supply voltages of about 700mV – 800mV, which is in super-threshold regions. The PDP of the bulk CMOS inverter is minimized at about 600mV, which is between near-threshold and super-threshold regions.

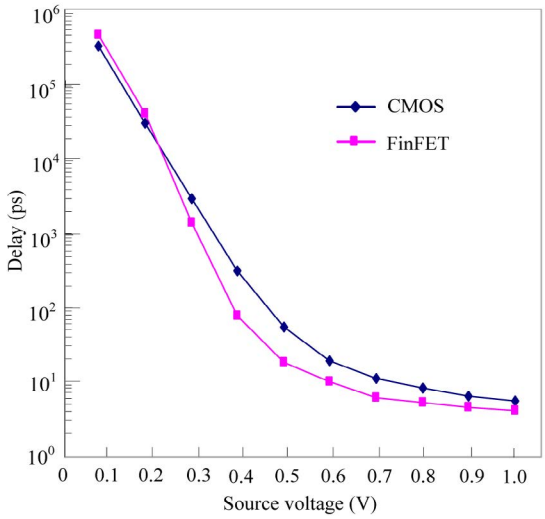

Figure 3. Propagation delay of the 32nm FinFET and bulk CMOS inverters

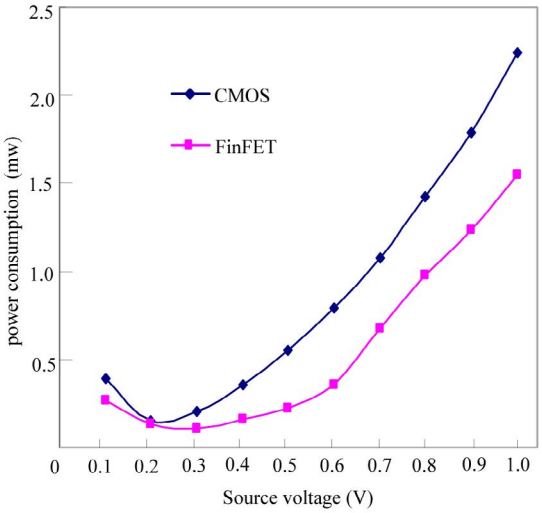

Figure 4. Power consumption of the 32nm FinFET and bulk CMOS inverters

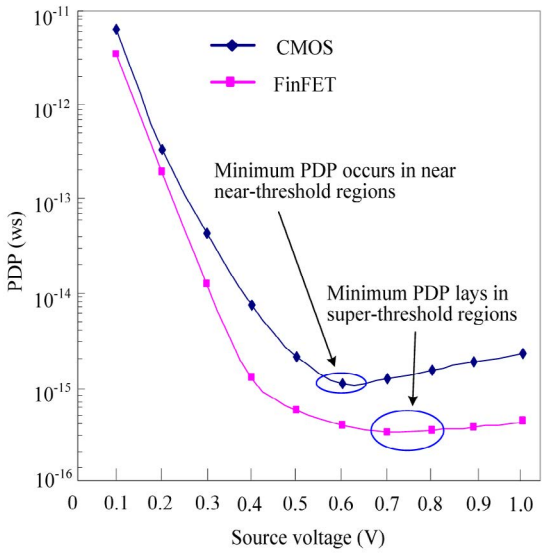

Figure 5. PDP of the 32nm FinFET and bulk CMOS inverters

3. FinFET flip-flops

A flip flop is one of important cells widely used in IC chips, and its performance plays a key role for whole circuits. The four typical flip flops, named as transmission-gate master-slave flip-flop, simplified static master-slave flip-flop, clocked CMOS master-slave flip-flop, and TSPC dynamic master-slave flip-flop operating on medium strong inversion regions are investigated in terms of settling time, propagation delay, power consumption, and power delay product.

A transmission gate master-slave flip-flop (TGMS) is shown in Fig. 6. The TGMS flip-flop is extensively used in standard cells of sequential systems because of its reliable performance and low power with simple structure [1]. The maximum speed of the flip flop is determined by the critical path (from *D* to *Q*). The setup time of the flip flop is sum of delay of three inverters and a transmission-gate. The propagation delay is sum of delay of an inverters and a transmission-gate.

As shown in Fig. 6, the TGMS flip-flop has large capacitive load in the clock node, resulting in large power dissipation in the clock network. One approach to reduce the capacitive load of the clock node is to eliminate the transmission gates in the feedback path, as shown in Fig. 7. In the simplified static master-slave flip-flop (SSMS), the two pairs of cross-coupled inverters in master and slave latches hold the state, which similar to the storage cell in memory arrays. The SSMS flip flop utilizes strong inverter in the critical path to meet timing constraint, while the inverter in the feedback path weakens the contention between critical path and feedback path effectively.

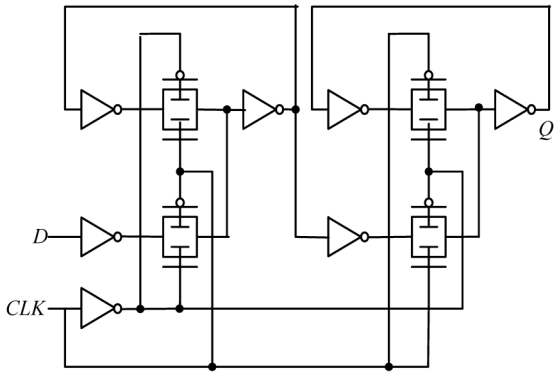

Figure 6. Transmission-gate master-slave flip-flop (TGMS)

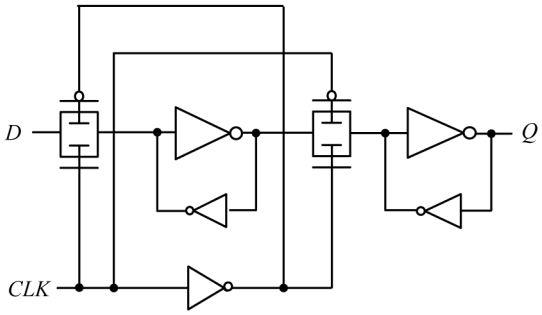

Figure 7. Simplified static master-slave flip-flop (SSMS)

A clocked CMOS master-slave flip-flop (C^2MOS) is shown in Fig. 8, which is implemented with static inverters and clocked inverters with tri-state function. The C^2MOS flip flop is not sensitive to clock overlapping phenomenon.

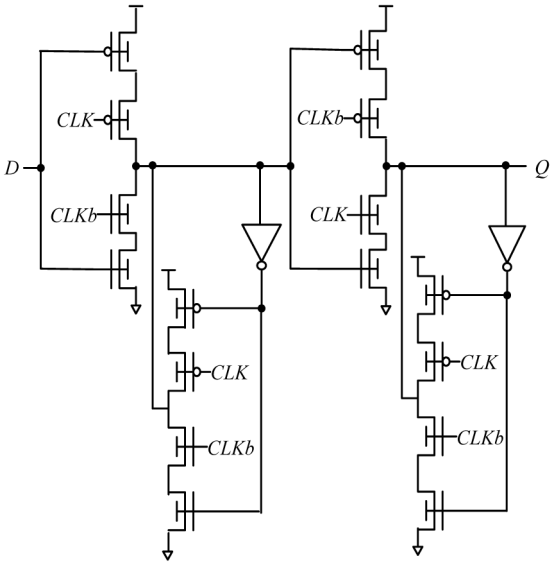

Figure 8. Clocked CMOS Master-Slave flip-flop (C2MOS)

True single phase clock master-slave flip-flop (TSPC) is an improved version of the C^2MOS flip flop, as shown in Fig. 9. The TSPC flip flop only use *clk*, and do not need *clkb*, and thus eliminate the influence of clock overlap. The design of the flip flop must ensure good CLK slope, and select the appropriate transistor size to avoid large signal noise.

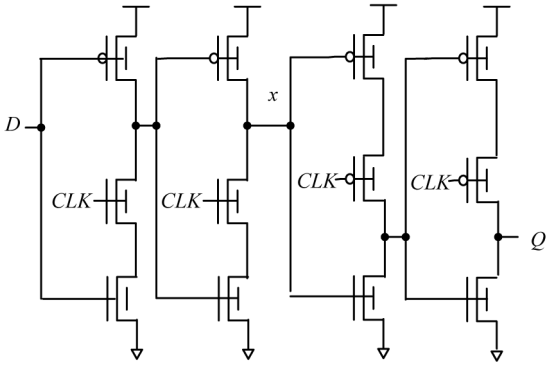

Figure 9. True single phase clock master-slave flip-flop (TSPC)

4. Simulation and results

The four typical flip flops operating on medium strong inversion regions are simulated in terms of settling time, propagation delay, power consumption, and power delay product. All circuits are verified with HSPICE at a 32nm BSIM-CMG FinFET technology.

Fig. 10 is the simulation results of the setup time of the four flip flops. The TGMS and SSMS flip flops have long setup time, because the status of the inverter ring must be changed in setup process of the flip flops. Compared with static flip flops, C²MOS and TSPC flip flops have a relatively small setup time, since the dynamic flip flops do not need to change the status of the inverter ring, and rely only on the parasitic capacitance of the circuit. The setup time of C²MOS and TSPC flip flops is only about 25% of the TGMS flip flop at 1.0V source voltage. As the source voltage scale down, the setup time of SSMS flip flop because of the contention between critical path and feedback path.

Fig. 11 is the simulation results of the propagation delay of the four flip flops. Similar to setup time, the TGMS and SSMS flip flops have long propagation delay. Compared with static flip flops, C²MOS and TSPC flip flops have a relatively small propagation delay, since the dynamic flip flops do not need to change the status of the inverter ring.

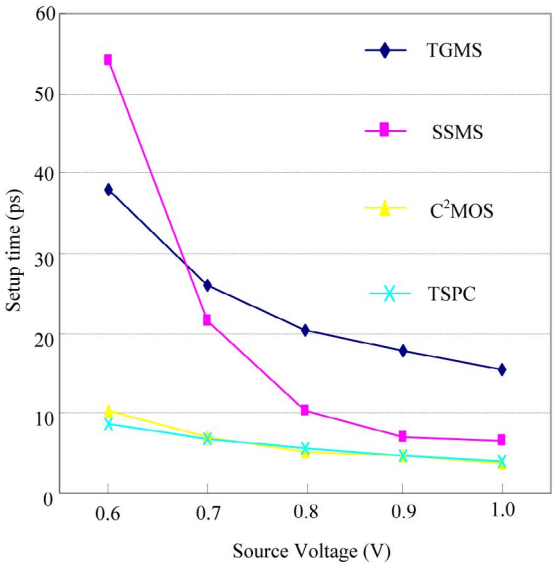

Figure 10. Setup time of four flip-flops

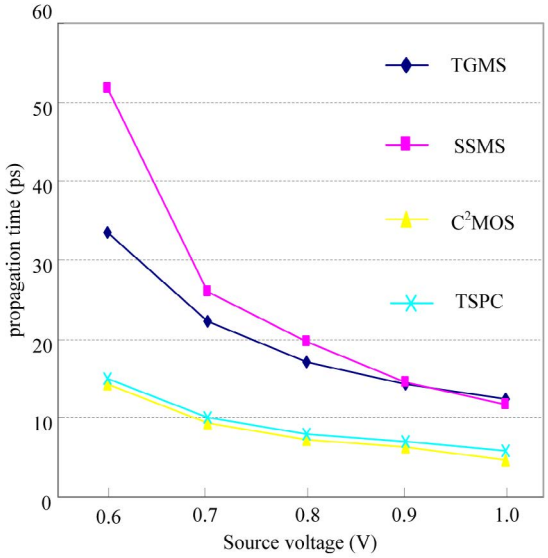

Figure 11. Propagation delay of four flip-flops

The propagation delay of C²MOS and TSPC flip flops is only about 40% of the TGMS and SSMS flip flops at 1.0V source voltage. As the source voltage scale down, the propagation delay of SSMS flip flop because of the contention between critical path and feedback path.

Fig. 12 is the simulation results of power consumption of the four flip flops. The power dissipation of the SSMS flip flop is largest, since the inverter ring with positive feedback in the SSMS flip flop forcedly changed resulting in a large energy dissipation, which is about four times of the TSPC flip flop. The C²MOS and TSCP flip flops have relatively small power consumption, and but is also sensitive to its source voltage. As the source voltage scale down, the power dissipation of TGMS and SSMS flip flops can be effetely reduced.

Fig. 13 is the simulation results of the power delay product (PDP) of the four flip flops.

The PDP of the SSMS flip flop is largest, since the inverter ring with positive feedback in the SSMS flip flop forcedly changed resulting in large power dissipation. The two dynamic flip flops have smaller PDP because their small power dissipation and delay. The PDP of C²MOS and TSCP flip flops is sensitive to its source voltage. As the source voltage scale down, the PDP of TGMS and SSMS flip flops can be effetely reduced.

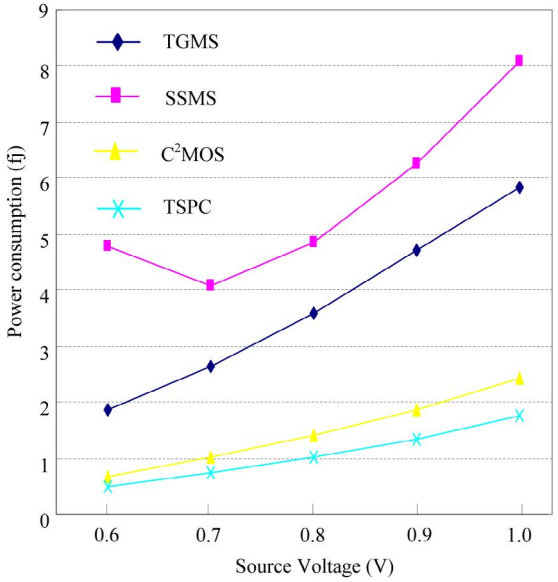

Figure 12. Power consumption of four flip-flops

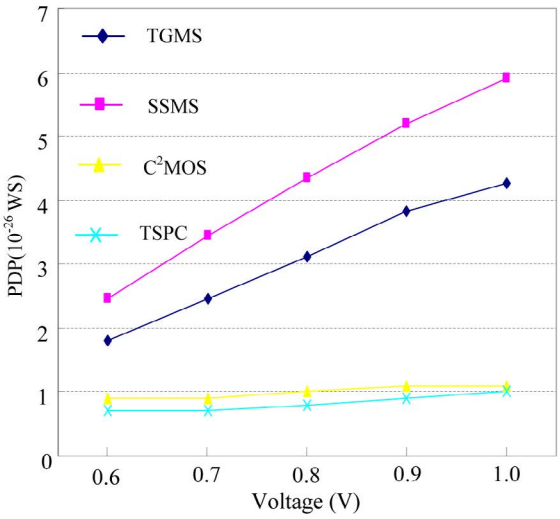

Figure 13. PDP of four flip-flops

5. Conclusions

In this paper, super-threshold computing of flip flops is presented. The four typical flip flops, named as transmission-gate master-slave flip-flop, simplified static master-slave flip-flop, clocked CMOS master-slave flip-flop, and TSPC dynamic master-slave flip-flop operating on medium strong inversion regions are investigated in terms of settling time, propagation delay, power consumption, and power delay product. The simulation results show that super-threshold FinFET flip flops attain about 38% power reduction with a penalty of only about 16% at 0.8 V source voltages.

Acknowledgements

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