Reliability evaluation of microelectronic device based on PoF

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Abstract
This paper puts forward a method to evaluate the reliability of microelectronic devices based on the theories of Physics of Failure (PoF), taking into account the different stress types and stress levels in application for microelectronic devices. Failure modes, mechanisms and effects analysis (FMMEA) is conducted to achieve the potential failure mechanisms and physics models based on the information of microelectronic devices during design, manufacture and application. The temperature, stress and electrical parameters under different stress levels are obtained by modeling and simulation. The matrix of time-to-failure of each unit is obtained by the failure physics models, cumulative damage theory and random sampling algorithm. Then the competing failure mode is applied to acquire the time-to-failure of MOS devices in working condition. The practice proves that this method is less time consuming, more efficiently, and costs less to evaluate the reliability of the microelectronic device under complex environments.

Key words: ASYMMETRIC FINGERPRINTING, OBLIVIOUS TRANSFER, MULTICAST COMMUNICATION

1. Introduction

Along with the rapid progress of microelectronic technology and integrate circuit industry, microelectronic devices have been applied to various aspects of society by virtue of simple process, high integration level, and good reliability [1-3]. And meanwhile, it presented new challenges to the reliability evaluation of microelectronic devices. Conventional reliability evaluation methods of the microelectronic device include: authentication and quality consistency check, accelerated life test, chip level reliability assessment, which costs much both of time and money [4,5]. Today the device reliability simulation evaluation based on Physics of Failure is being widely researched. Texas Instruments researched the thermoelectric effect evaluation of microelectronic devices by simulation method. University of Southern California and University of California, Berkeley in American researched the method of proceeding simulation evaluation with the SPICE software. CALCE center at the University of Maryland researches that how to evaluate the lifetime of microelectronic devices considering only single failure mechanism of chips.

However, through analysis, these arithmetic has two defects: (1) the analytic target of these method is the chip and therefore only the failure mechanism of the MOS structure inside the chip is considered, while the failure of packaging and interconnection is not which is also frequent in actual use; (2) These methods are specific to reliability issues of single failure mechanism under single stress level, which is different from the actual using environmental condition of microelectronic devices.

For this purpose, this paper presents a reliability simulation assessment method which considers the complex stress of actual use, and multiple failure mechanisms of both chips and packaging.

2. Basic procedure

Reliability evaluation by simulation for microelectronic device based on PoF synthetically considers the complex stress (multiple stress levels and multiple stress types) of actual using conditions, and multiple failure mechanisms (including chip level and packaging level). The main flows are: (1) Microelectronic devices data collection of design, manufacture, and use; (2) Failure mode, mechanisms, and effects analysis (FMMEA), to obtain the potential failure mechanism and failure physics model; (3) Analysis of stress simulation: modelling the MOS device includes chip layout and packaging, obtain the temperature, stress-strain, and electrical performance parameters of the failure physics model through simulation analysis; (4) Failure prediction: obtain the failure time matrix of each simulation units by stress damage analysis, cumulative damage analysis, and parameter random simulation; (5) Reliability assessment: applying competing failure mechanism to acquire the time to failure of MOS devices while taking multiple failure mechanisms into account, as shown in the Figure 1.

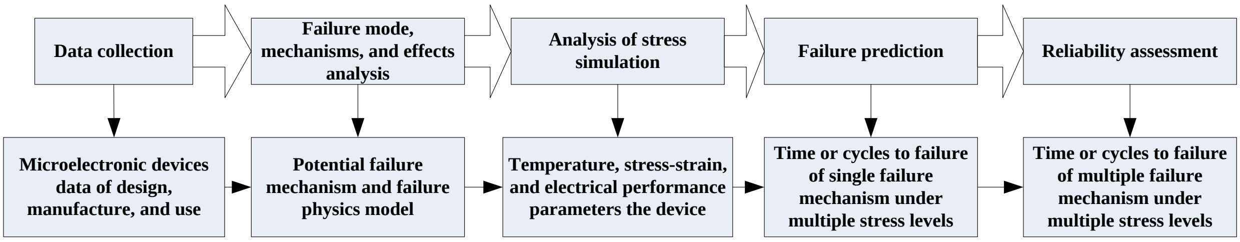


Figure 1. Flow chart of reliability evaluation by microelectronic device simulation based on PoF

3. Data collection

Before simulation analysis and failure prediction of the microelectronic device, we need to know about the research object, including design flow, manufacturing process, and environmental conditions of actual use. Also, the accuracy and integrity of data collection is closely related to the subsequent simulation evaluation. So, as a key step of the microelectronic device simulation evaluation, data collection lays the foundation of subsequent simulation analysis. As shown in Table 1, the main contents and approaches are as follows:

Table 1. Data collection contents and approaches

Contents	Collecting approaches	Remarks
Structure parameters	1 Data sheet of devices 2 Design document of devices	—
Electrical performance parameters	1 Calculate by Equation 2 Empirical value of design	—
Environmental stress parameters	Operating environment history of MOS devices of similar products	—
Other parameters	Pertinent literature	Power dissipation

4. Failure mode, mechanism, and effects analysis

Combining FMMEA with PoF, the potential failure mechanisms and models inside the failure modes of the microelectronic device can be confirmed and the priority of failure mechanism can be divided [6].

For microelectronic devices, we first need to define the system, divide it into 3 levels: packaging, bonding, and chip by structure.

Then, make a list of all potential failure modes according to different level, and ascertain the failure physics models. Finally, rate the potential failure mechanisms, and ascertain the potential failure mechanism with the highest priority during the operating of the microelectronic device as the follow-up key analysis object.

5. Analysis of stress simulation

Analysis of stress simulation includes two parts: modeling and analysis, as shown in Figure 2.

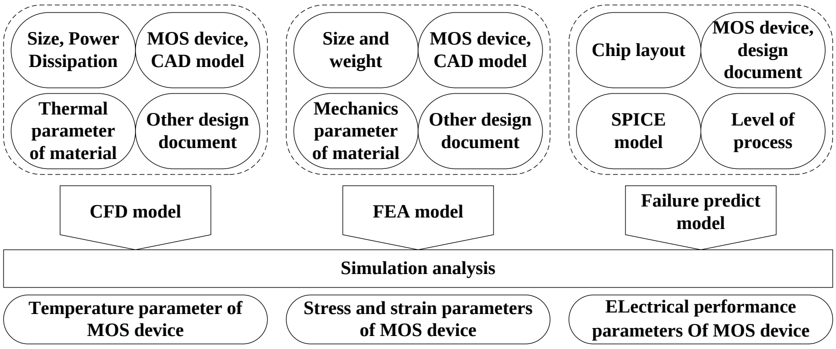


Figure 2. Flow chart of analysis of stress simulation

5.1. Modelling

Microelectronic device modelling includes CFD model, FEA model, and failure prediction model.

CFD model is a kind of numerical heat transfer model which is built by combining structure, thermal property and power dissipation of the device. The CFD model completely describes the geometric construction, heat production, and heat-transfer characteristic of the microelectronic device, and the accuracy of it is the key point of whether the local temperature of the microelectronic device can be obtained accurately.

FEA model is a kind of finite element model which is built by combining structure, mechanical property of the material, and weight of the device. The FEA model completely describes the geometric construction, and mechanical transmission characteristics of the microelectronic device, and the accuracy of it is the key point of whether the local stress-strain of the microelectronic device can be obtained accurately.

The failure prediction model is built by combining packaging and chip layout, and it completely describes the geometric construction, and Circuit features. The accuracy of it is the key point of whether the electric performance parameters of the microelectronic device can be obtained accurately.

5.2. Simulation analysis

Stress parameters refer to the related parameters involved in the failure physical models which correspond to common failure mechanism, such as temperature, stress, strain, moisture, current of the microelectronic device. Temperature simulation analysis, vibration response simulation analysis, and electric performance parameters simulation analysis should be carried out before conducting the failure prediction and reliability assessment, to obtain relevant stress parameters as input for the follow-up failure prediction calculation.

6. Failure prediction

Failure prediction refers to combining the high priority potential failure mechanism obtained by FMMEA analysis, using the corresponding failure physical model and stress simulation analysis results, carrying out stress damage analysis, cumulative damage analysis, and parameter randomize simulation, obtaining failure time matrix of the simulation units of single failure mechanism and multiple stress levels. The flow chart is as shown in Figure 3.

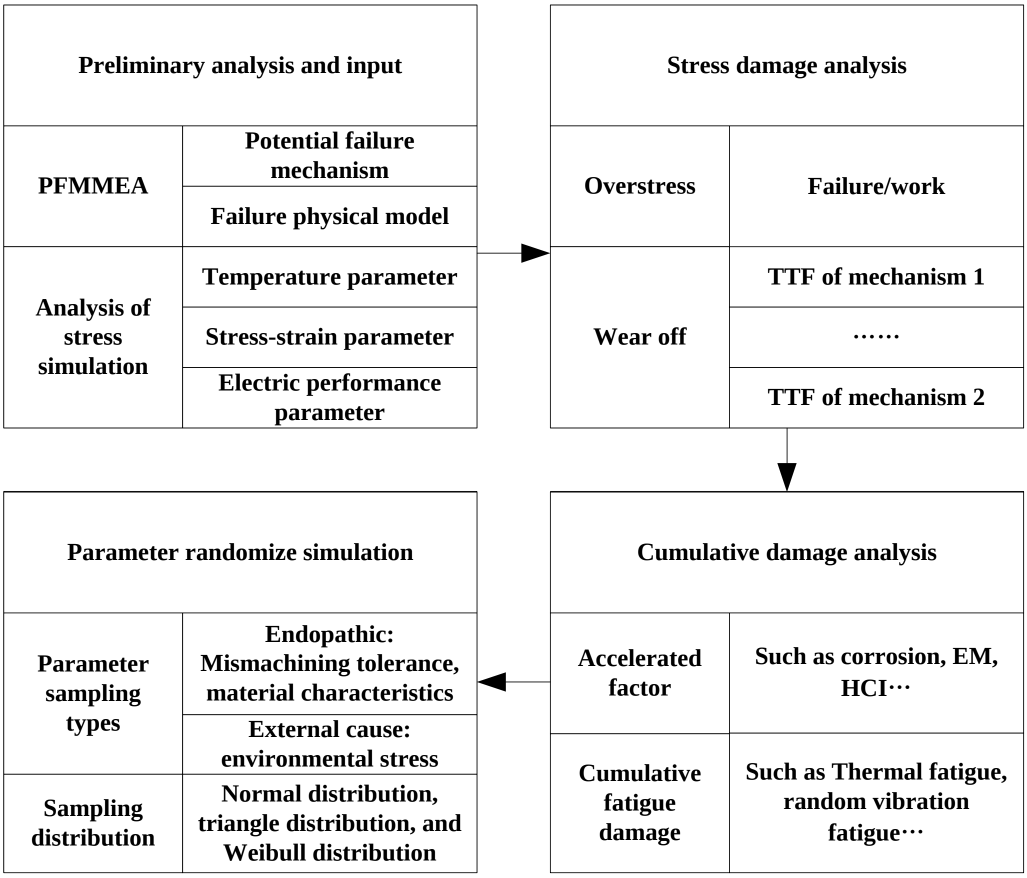


Figure 3. Flow chart of failure prediction

6.1. Stress damage analysis

When the temperature, moisture, stress, strain, and corresponding electrical performance parameters of the microelectronic device are obtained by analysis of stress simulation, the stress damage computing using failure physical models of different potential failure mechanism can be conducted.

For overstress failure mechanism, just judge whether the simulation unit can bear the given stress according to the failure physical model. If the unit can, then continue the follow-up analysis, otherwise declare it a failure. For wear off failure mechanism, calculate the time or cycles to failure of each simulation unit under a certain stress level for each failure mechanism by failure physical models. It should be pointed out that stress damage analysis need to be done separately according to the different environmental stress levels in actual use, to prepare for the follow-up cumulative damage process.

6.2. Cumulative damage analysis

Cumulative damage analysis, based on the stress damage analysis, which combined with different environmental stress sequence during life time, separately make use of accelerated factor method and cumulative damage theory to compute. Then convert cycles to time, the time to failure of each simulation units of the microelectronic device under multiple stress level of single failure mechanism can be obtained.

6.2.1 Accelerated factor method

Accelerated factor (AF) refers to the ratio of the life feature under high stress level to life feature under normal stress level, which originates in accelerated test, to describe the degree of acceleration. When AF is larger than 1, it means that increasing stress S shortens the life of the product [7]. Its definition is:

$$AF_i = \frac{t_{p,0}}{t_{p,i}} \tag{1}$$

Where $t_{p,0}$ refers to life feature under stress level S_0; and $t_{p,i}$ refers to life feature under stress level S_i.

Taking advantage of the AF from accelerated test, convert the multiple stress levels in actual use to single stress level to evaluate. Then calculate the threshold cycles under life profile with the time to failure of simulation under single stress level and in turn obtain the time to failure of the product under actual use condition. For instance, in figure 4 there is a life profile of two temperature level, T1 and T2. According to Equation (2), it can be converted into single stress level (assumed to be T0) and obtain the corresponding time.

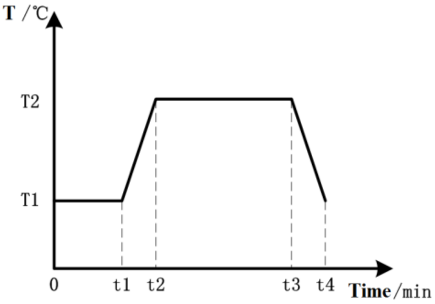


Figure 4. Profile example of AF method

$$t\_trans = t1 \times AF(T1) + \int_{t1}^{t2} AF(T(t))d(t) + (t3 - t2) \times AF(T2) + \int_{t3}^{t4} AF(T'(t))d(t) \tag{2}$$

Where *t_trans* refers to the equivalent time after convert to temperature level *T0*; *AF(Ti)* refers to the AF of temperature level *Ti* to temperature level *T0*, which can be obtain by definition and specific failure physical model. $T(t)$ and $T^{'}(t)$ are the temperature function of time during the changing sections.

6.2.2. Cumulative damage low method

There are many cumulative damage models, such as linear cumulative model, bilinear cumulative model, nonlinear cumulative model, and other models. Taking the interaction between different loading sequence in to consider, the Corten-Dolan cumulative damage low are adopted to solve the solder joint thermal fatigue and Random vibration fatigue problems. The cumulative damage equation is as follows.

$$N_g = N_1 / [\sum_{i=1}^{m} \alpha_i (\frac{\sigma_i}{\sigma_1})^d] \tag{3}$$

Where *Ng* is the fatigue life under multilevel stress; N_1 is the constant amplitude fatigue life under the highest stress level of the loading spectrum; σ_1 is the maximum stress of the multilevel stress spectrum; α_i is the percentage of cycle number of the alternating stress σ_i in the total cycles of the loading spectrum; m is the stress level, d is a constant which values 4.8 for high-strength steel and 5.8 for others.

According to the random vibration PSD spectrum, the vibration response (the location of the maximum stress point of the pin and the statistical average frequency) of the microelectronic device under each stress level by vibration response simulation analysis. Using the three interval method [8] which is based on Gaussian distribution and proposed by Steinberg, for stress levels spectrum, the analysis process is as follows:

(1) Computing the statistical average frequency (stress velocity / stress) of response under each stress level;

(2) Computing the cycle numbers *n1*、*n2* and *n3* under level 1σ、2σ and 3σ based on expectation (working) life and statistical average frequency;

(3) Look up for *N1*、*N2* and *N3* based on S-N curve;

(4) Computing the fatigue life.

6.3. Parameter random simulation

The failure of the microelectronic device is a synthesize result of external cause and internal cause. External cause refers to the environmental conditions during the operation. Internal cause includes the packaging, material of the chips, structure size deviations during the manufacturing process. Therefore, the potential external and internal cause which may lead to failure must be analyzed comprehensively during the reliability simulation assessment of the microelectronic device to obtain a more comprehensive assessment result. The choices of the parameter distributions [9-12] are as shown in Table 2.

Table 2. Parameter distribution choices

Distributions	Environmental stress [4~6]	Material property [7,8]	Structure size[8]
Normal distribution	√	√	√
Weibull distribution	√		

Exponential distribution		√	
Triangular distribution		√	√

According to Table 2, carry out Monte Carlo sampling for each failure physical model parameter to obtain the failure physical model parameter matrix:

$$\theta=\begin{bmatrix}\theta_{11},\theta_{12},\cdots\theta_{1n}\\ \theta_{21},\theta_{22},\cdots\theta_{2n}\\ \cdots\\ \theta_{m1},\theta_{m2},\cdots\theta_{mn}\end{bmatrix} \qquad (4)$$

Where m refers to the number of parameters, and n refers to the sampling times.

Put each column in the corresponding failure physical model to compute and obtain large sample of time to failure or cycles under single failure mechanism. Repeat this for each failure mechanism to obtain the matrix for different failure mechanism under single stress level as follows:

$$TTF=\begin{bmatrix}TTF_{11},\cdots,TTF_{1i},N_{1(i+1)},\cdots,N_{1n}\\ TTF_{21},\cdots,TTF_{2i},N_{2(i+1)},\cdots,N_{2n}\\ \cdots\\ TTF_{k1},\cdots,TTF_{ki},N_{k(i+1)},\cdots,N_{kn}\end{bmatrix} \qquad (5)$$

Where *k* means that there are *k* different potential failure mechanisms considered. If a failure mechanism doesn’t exist for a simulation unit, the numbers in corresponding row value 0.

For each element, by proceeding damage cumulative method, the time to failure matrix of each simulation unit under multilevel stress can be obtained.

$$t=\begin{bmatrix}t_{11},t_{11}\cdots,t_{1n}\\ t_{21},t_{21}\cdots,t_{2n}\\ \cdots\\ t_{k1},t_{k1}\cdots,t_{kn}\end{bmatrix} \qquad (6)$$

7. Reliability evaluation

The reliability evaluation of microelectronic devices using the time to failure matrix obtained by failure prediction, take multiple failure mechanisms, and take advantage of the competing failure modes (as shown in Equation (7)).

$$T_i=\min(t_{1i},t_{2i},\cdots,t_{ki}) \qquad (7)$$

The obtained time to failure matrix of the microelectronic device of multiple failure mechanisms under multiple stress levels is as:

$$T=[T_1,T_2,\cdots T_n] \qquad (8)$$

Carry out parameter fitting and test of goodness of fit, obtaining the failure probability density function *f(t)*, and calculate the reliability. The MTTF (Mean time to failure) can be obtained by Equation (9).

$$MTTF=E(t)=\int_0^{+\infty}tf(t)dt \qquad (9)$$

8. Case study

In this paper, we select a MOS device with plastic dual inline-pin (DIP) package which provide the system designer with direct implementation of the NOR function. We will depict the process of reliability evaluation by simulation in detail with this device.

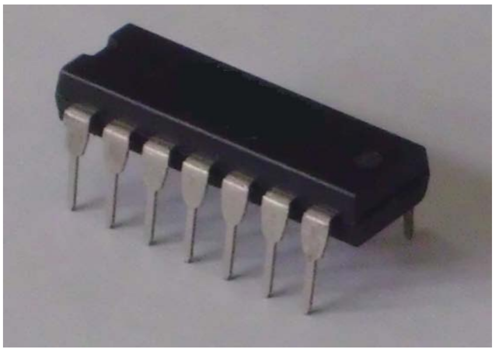


Figure 5. The MOS device which is applied in case study

8.1. Parameter extraction

At first, it’s necessary to extract the parameters of structure and operation conditions and so on. According to datasheet, design files and historical data, the parameters can be extracted.

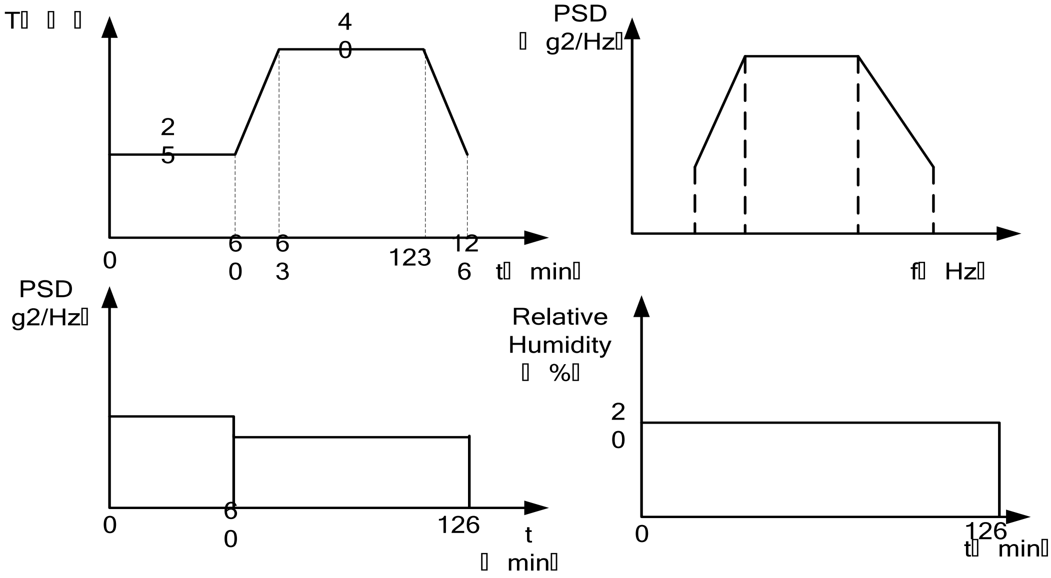


Figure 6. The operation profile of the MOS device

Table 3. Parameters of profile for random vibration

No.	Frequency（Hz）	PSD（g2/Hz）
1	5	0.0266
	75	0.4
	200	0.4
	2000	0.004
2	5	0.0133
	75	0.2
	200	0.2
	2000	0.002

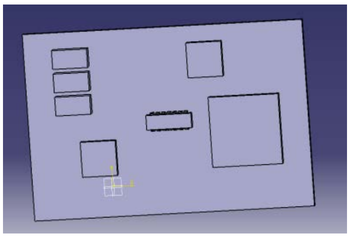
8.2. Failure Mode, Mechanism and Effects analysis (FMMEA)

In this paper, the MOS device is divided into three general classes firstly: package, interconnects and die. Considering the failure that happened before, the failure modes, mechanisms are determined.

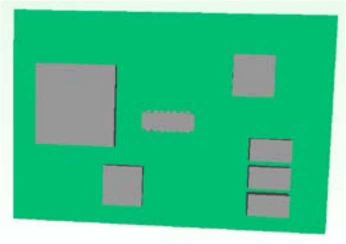
According to the results of FMMEA, the potential failure mechanisms which have a greater impact on the performance of the specific MOS device include: Solder Joint Thermal Fatigue(SJTF), Random Vibration Fatigue(RVF), Corrosion, Gate-oxide Time Dependent Dielectric Breakdown (TDDB), Electro –Migration(EM) and Hot Carrier Injection (HCI). So in the following steps, we focus on these six failure mechanisms and evaluate the reliability with them.

8.3. Analysis of stress simulation

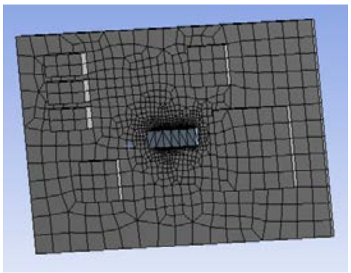
According to the basic parameters, the CAD, CFD and FEA models are built. We develop researches on thermal analysis, random vibration analysis and electrical parameters analysis and results are soon obtained.



a) CAD model



b) CFD model



c) FEA model

Figure 7. Three models of MOS device located in the middle of board and PCB

8.4. Stress damage analysis and Cumulative damage analysis

In terms of the seven potential failure mechanisms, we divide them into depletion-type and overstress-type. It is only need to confirm whether it is strong enough to stand the specific stress under operation conditions for overstress-type while it is necessary to consider the cumulative damage for depletion-type.

According to the result of FMMEA, potential failure mechanism of shock is the only overstress-type and the stress is not enough to make device failure.

The next work is to calculate the time-to-failure or cycle-to-failure of the six potential failure mechanisms for each simulation unit in Table 4.

After this, we develop the cumulative damage analysis. We got the cumulative damage AF Formula such as:

$$AF_i = \frac{MTTF_0}{MTTF_i} = \left(\frac{T_0}{T_i}\right)^m \exp[\frac{Ea}{k}(\frac{1}{T_0}-\frac{1}{T_i})] \qquad (10)$$

And we used formula (2) to calculate the TTF for the cumulative damage, TTF for EM cumulative damage in is 8392h.

For the RVF, we used Formula (3) to calculate the cumulative damage Cycle-to-failure as 8.2437e+009 cycles.

Table 4. Time-to-failure or Cycle-to-failure of the failure mechanisms

No.	Failure Mechanism/Stress		Time-to-failure/Cycle-to-failure
1	EM	Temperature 25℃	11707h
		Temperature 40℃	4519.6h
2	TDDB	Temperature 25℃	11360h
		Temperature 40℃	9587.3h
3	HCI	Temperature 25℃	11857h
		Temperature 40℃	10892h
4	Corrosion	Temperature 25℃	9588.2h
		Temperature 40℃	4410.1h
5	RVF	Stress Level 1	7.8059e+009 cycles
		Stress Level 2	8.5125e+009 cycles
6	SJTF		3.7467e+003 cycles

8.5. Parameter randomize simulation

Considering the uncertainty of parameters, Monte –Carlo(MC) approach is widely used. The distribution types of the different parameters of Failure physical model are given as Table 5.

Table 5. Distribution of the parameters

Failure Mechanism	Parameter	Distribution
Solder Joint Thermal Fatigue	LD: LENGTH	Triangular
	h: Solder Height	Triangular
	ΔT: Cyclic Temperature Swing	Weibull
	Tsj: Mean Cyclic Temperature of the Solder in Degrees C	Normal
	αc and αs: Coefficients of Linear Thermal Expansion for Component and Substrate	Triangular
Random Vibration Fatigue	B: Length of the PCB Edge Parallel to the Component Located at the Center of the Board	Normal
	L: LENGTH	Triangular
	t: Thickness of PCB	Normal
	fn: Minimum Natural Frequency	Normal

Electromigration	W: Width of Interconnects	Normal
	d: Thickness of Interconnects	Normal
	T: Temperature	Normal
	j: Current Density	Triangular
TDDB	Eox: Oxide Field	Triangular
	T: Temperature	Normal
HCI	T: Temperature	Normal
Corrosion	RH： Relative Humility	Normal
	T: Temperature	Normal

In the following step, we develop the MC to obtain the vector of TTF for EM. At first, get the 10000 samples of uncertain parameters (W, d, T and j) by monte carlo approach.

$$\theta = \begin{bmatrix} 0.790114832, 0.798267848, 0.79834634, 0.800647454, \cdots, 0.799123104 \\ 0.981133085, 1.007929821, 1.008361467, 1.000597051, \cdots, 1.015567806 \\ 55.84119123, 56.5393662, 55.23497947, 56.09943779, \cdots, 55.60634757 \\ 0.298663927, 0.302170728, 0.301507547, 0.299965692, \cdots, 0.299706913 \end{bmatrix}$$

Then according to PoF model, the vector of TTF is

$$TTF = [11297.991, 11113.816, 12055.017, 11445.712, \cdots, 11954.772]$$

For each element of vector of TTF, calculate the time-to-failure considering the cumulative damage under the profile given in section 8.1.The result is,

$$t = [6312.42, 6209.51, 6735.38, 6394.95, \cdots, 6679.37]$$

Calculate the TTFs of other potential failure mechanisms and form the matrix of TTF for each simulation unit,

$$t = \begin{bmatrix} 6312.42, & 6209.51, & 6735.38, & 6394.95, \cdots, & 6679.37 \\ 8944.57, & 8418.34, & 9010.22, & 8262.84, \cdots, & 9900.97 \\ 11396.04, & 11361.27, & 11360.94, & 11351.17, \cdots, & 11357.64 \\ 9344.20, & 10396.72, & 9835.80, & 9241.89, \cdots, & 9546.54 \\ 6758.65, & 6825.83, & 6826.47, & 6845.44, \cdots, & 6832.87 \\ 7835.58, & 7742.86, & 7877.52, & 7889.73, \cdots, & 7781.90 \end{bmatrix}$$

8.6. Reliability Evaluation

Calculate the vector of TTF of MOS devices using competing failure mode and the result is

$$T = [6312.42, 5277.05, 6735.38, 6394.95, \cdots, 6679.37]$$

The data is well fitted as the Weibull distribution and the TTF of MOS device is 6415.9h under the operation conditions given in section 8.1.

9. Conclusion

The speeding developing of technique raises the integration and enlarges the applied range of the microelectronic device, which bring new challenge to its reliability evaluation. Traditional evaluating methods are time consuming, high cost, and update slowly. Meanwhile the existing simulation evaluation methods are not able to evaluate the reliability of packaging failure or complex stress conditions.

Therefore, this paper presents a reliability evaluation method, which studies microelectronic device based on PoF. Combining the design, manufacture, and operating data of the microelectronic device, this method evaluates the reliability of the microelectronic device of multiple failure mechanisms under complex stress conditions by FMMEA, analysis of stress simulation, failure prediction, and reliability evaluation. The method can evaluate the reliability of the microelectronic device effectively while it is less time consuming, more efficient, and costs less.

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