Digital Signal Processing Algorithm of High Speed Digital Circuit in Physical Layer

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Abstract
In this paper, the author studies about the digital signal processing algorithm of high speed digital circuit in physical layer. At present, the digital signal processing has applied extensively in many subjects such as communications, radar, sonar, speech and image processing etc. In order to solve the problem of performance degradation which arises from sequence truncation in many digital signal processing occasions, this paper prompts an algorithm for the digital signal processing algorithms of high speed digital circuit in physical layer. The experiment result shows that the performance can be improved by using this algorithm.
Key words: DIGITAL SIGNAL PROCESSING ALGORITHMS; HIGH SPEED DIGITAL CIRCUIT; PHYSICAL LAYER.

1. Introduction

Digital Signal Processing is one of the subjects expanding rapidly in the field of information science during the past" several decades. At present, it has applied extensively in many subjects such as communications, radar, sonar, speech and image processing etc. General speaking, there are 3 ways to implement the digital signal processing algorithms, programming DSP for general purpose, ASIC and DSP chipset with invariable function for special purpose, FPGA that can be programmed by user. With the development of micro-electronics technology, realizing digital signal processing with FPGA develops rapidly, more and more, FPGA is used in the arithmetic of front-end digital signal processing in place of ASIC and PDSP.

Yan's [1] paper mainly probes into the realization of digital signal processing based on FPGA. At first the fundamental theory of digital signal processing and the DFT algorithm are expounds, then radix-2 FFT and the characteristic of DIT FFT are discussed. In Baldwin's [2] paper, the description method and style of hardware description language and its development environment MAXPLUSII are detailed. On the basis of that, the high level design method of integrated digital system and the partition of design level of digital system are discussed; the top-down design strategy and the high level synthesis method of digital system are also detailed. After doing that, the paper pointed out the universal architectures of the high-speed real-time signal processing system and described how to implement them. Since FFT plays an important role in digital signal processing, implementing FFT with FPGA is presented and the total realization graph is designed in Ohtani' s paper [3]. For improving speed and decreasing computing complexity, high efficiency multiplier algorithm is used to realizing twiddle factor multiplier of butterfly processing unit.

In order to solve the problem of performance degradation which arises from sequence truncation in many digital signal processing occasions, Lai's paper

[4] proposes a lot of improved methods based on 'all-phase digital signal processing', involving the fields of digital filtering, spectrum analysis, signal reconstruction and statistical signal processing etc.

The general calculating formula for the coefficients of all-phase equivalent FIR filter under arbitrary orthogonal transform is deduced in Takahashi H's paper [5]. The interpolation method based on convolution-window's spectrum function and cyclic shift figure method are respectively applied to deduce the frequency response function of all-phase filter in DFT domain, which can interpret the reason that all-phase design method with single window is fit to design those filters with discontinuous frequency character. Moreover, quantitative analysis on the computation complexity and flexibility of all-phase filter's 5 equivalent structures is given in details. Secondly, both the changes of determined signal's waveform & spectrum and the changes of stationary random signal's mean value & variance after all-phase pre-processing are studied in Semykina A S's paper [6].

A novel 'even symmetric' frequency sampling mode is introduced. By this mode, two kinds of all-phase filter design methods based on double phase-shifting combination and frequency character compensation are respectively proposed. In addition, the technique of frequency response masking and the technique of all-phase filtering based on even symmetric frequency sampling are incorporated, so the problem of controlling boundary frequency bands is solved. Moreover, the notch filter whose notch frequency point can be shifted arbitrarily is successfully designed. To overcome the deficiencies of big waveform distortion and Gibbs effect in conventional discrete Fourier reconstruction, a novel all-phase Fourier reconstruction algorithm is proposed in Kabuo H's paper [7]. It is also pointed that the all-phase Fourier reconstruction and all-phase FIR filter design are uniform indeed. Both of them reflect that all-phase method is fit to discontinuous signal's processing. Lastly, the mechanism of all-phase FFT (apFFT) spectrum analysis is deeply studied. The viewpoint that 2 sub-spectrums can adaptively adjust the performance of apFFT's spectrum is proposed and proved. Four basic properties of apFFT spectrum analysis are discovered, among which the property of square relation between the apFFT spectrum amplitude and the conventional FFT spectrum amplitude for single-frequency complex exponential sequence as well as the property of 'phase invariant' are strictly proved. Several correcting spectrum methods based on apFFT are expatiated, among which all-phase time-shifting phase difference correcting method has the highest precision. This paper also applies apFFT and the corresponding correcting spectrum methods into many aspects such as phase meter design, feeble signal detection, harmonic analysis of power system, radar velocity measuring, laser wavelength measuring etc.

2. The Basic Model and Framework

It has been 30 years ever since the Digital Signal Processor (DSP) came into being, which accelerates the process of digital signal processing from the theory to the practical use. Furthermore, it becomes the basic component used in communications, computers, and consumer electronics. With the rapid development and popularization of DSP technology, more and more people are recognizing and familiar with it and use it. Since communications technology, electronic technology and network technology are developing quickly, in order to meet the demand of this rapid development, it is necessary to update and improve professional electric communications courses and experiment instruments in universities. As a result, the related courses construction in the higher education as well as their experiment teaching standards should be further improved. Consequently, it is more important to make students themselves grasp the new technology of the digital signal processors and improve their comprehensive design abilities.

Although there are so many kinds of DSP products in the market, there are few ideal products designed for college student practical experiments. In order to improve their practical competence in major fields and make them understand the basic theory and related application systemic concept mode of DSP, an integrated digital signal processing experiment system closely associated with the experiment teaching outlines is designed and implemented.

Ohtani K's paper [8] analyzes the integrated experiment system hardware and software technology for the realization in a new structure of DSP+CPLD, resolves some key technology problems applied in the practical process of the integrated experiment system and completes hardware system platform for the integrated experiment system according to the demand, moreover, It creates and designs the related testing codes, arithmetical programs and comprehensive experiment programs based on this hardware platform. The idea of the modularization design is infused in the systemic hardware, and the realization methods of concrete circuit design in many modules, such as the hardcore module, the memory module, the lattice diagram liquid-crystal display module, the speech processing module, the network control module, the boot loader module and programmable logic device are concluded.

Totally speaking, in hardware design process of high speed digital circuit in physical layer, the key technologies are:

1. Design of the integration of all logic control circuit based on the Complex Programmable Logical Device (CPLD), and use of CPLD in place of the universal device to overcome the complex and flexible defects so as to shorten its development cycle and increase the system flexibility and expansibility.

2. Use of the jumper mode of network controller RTL8019AS to design the network control module, which offers data transmission service of the digital signal processing experiment system network and sets up the scheme of network application.

3. Resolutions of two important problems by single-chip: one is the DSP's Boot loader and the other is the data transmission between DSP and PC.

4. Deployment of Multi-channel Buffered Serial Port (MCBSP) of DSP as the universal input and output port and realization of Universal Asynchronous Receiver and Transmitter (UART)communications through simulated time-sequence control without other external circuit for the complexity reduction of the circuits. In the second section, flow chart of software development of the TMS320VC5409 DSP, the composition ways and patterns of the interrupt vector table files and DSP command files are given. Furthermore, programming operation of FLASH memory is considered, and the software design of the speech module and liquid-crystal Display module are discussed. The data transmission between PC and the experiment system is completed and boot load method of the DSP host port interface controlled by the single-chip and its program design realization plan is also important to the design. The figure 1 shows the flow chart of digital signal processing.

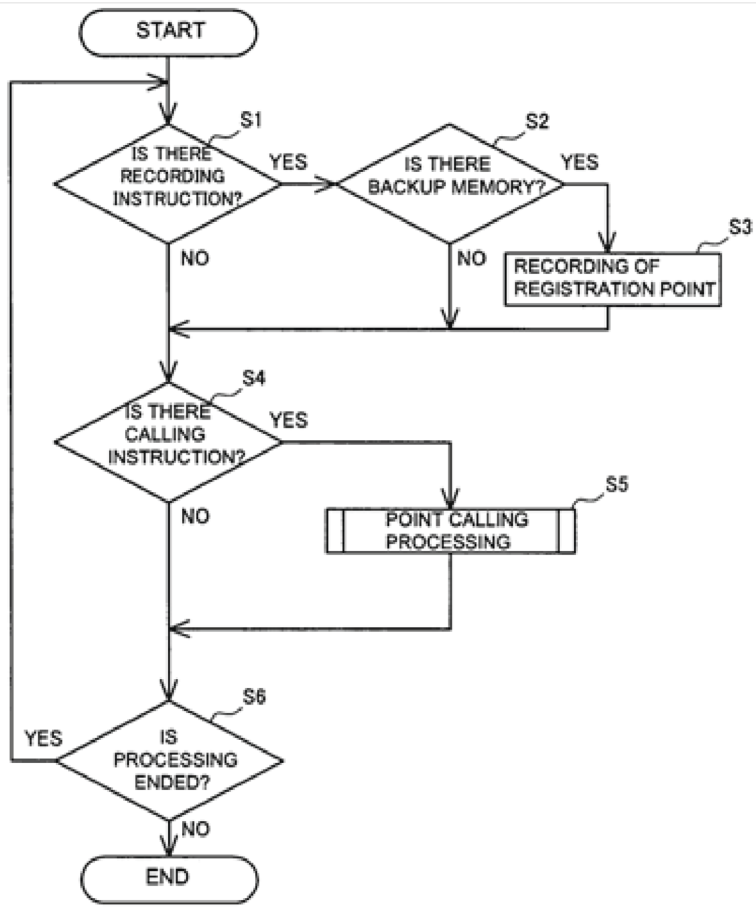

Figure 1. The flow chart of digital signal processing

In software design process of high speed digital circuit in physical layer, the key technologies are:

1. Composition of testing code in allusion to respective modules of the hardware circuit and check of the working status of the hardware circuits.

2. Realization of the digital signal processing algorithmic programs and proposal of the reference demonstrations of the various algorithms for the users.

3. Completion of the integrated experiment system programs and the reference experiment examples for the users.

3. The Algorithm and FPGA Implementation

Digital signal processing is to use a computer or special processing equipment to collect, transform, filter, valuate, enhance, compress and identify the signal, to obtain the signal form met the needs. The essential of the digital signal processing technology is to convert the analog signal or some signals in real life into digital signals and carry out corresponding processing for the converted digital signals.

Figure 2 is a simplified diagram of digital signal processing system. This system first transforms the analog signals into digital signals, and after digital signal processing, and then converts them into analog signals for output. In which, the role of anti-abasing filter is to remove the component higher than the folding frequency (its value is equal to half the sampling frequency) in the input signal x (t), to prevent signal spectrum abasing.

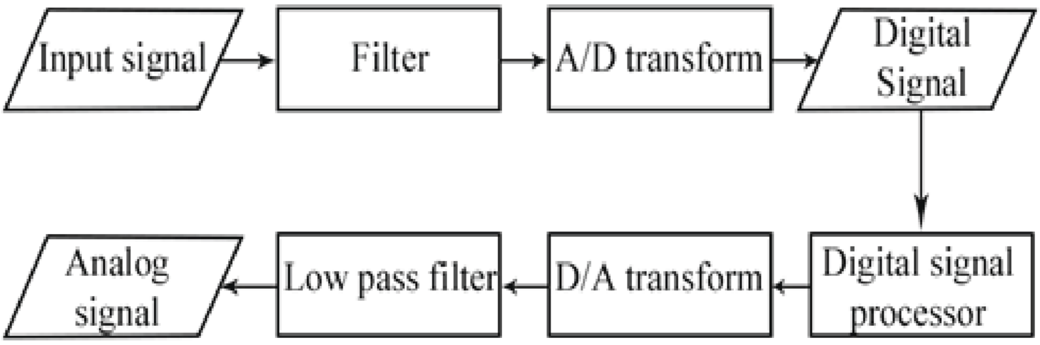

Figure 2. The flow chart of design process

Subsequently, through sampling and D/A transform, the signal is changed as digital signal x (n). The digital signal processor will process the x (n) and obtain output digital signal y (n), which will be converted into analog signal through D/A converter and through a low pass filter to filter out the unwanted high frequency components and finally output smooth analog signal y (t). FPGA can not only solve the electronic system miniaturization, low power, high reliability, and other problems, and its development period is short, software development cost is smaller chip price is continuously reduced, which makes it share more and more markets, especially for the product demand with small quantity and various types, FPGA is preferred. Another important reason of FPGA popularity is that IP (intellectual property) is increasingly concerned, and the functional blocks with IP core is widely used in the ASIC design platform. More and more designers adopt design reuse to modular the system design, which brings speed and convenience to the design, also makes each designer can make full use of software code to increase development efficiency, reduce time to market, reduce development costs, shorten development cycles, and reduce disk. The basic equation of the algorithm is shown in the following equation (1):

$$C(\mathrm{x}) = C^0 + C^1(\mathrm{x}),\ e(\mathrm{x}) = e^0 + e^1(\mathrm{x}),\ \eta(\mathrm{x}) = \eta^0 + \eta^1(\mathrm{x}),\ \rho(\mathrm{x}) = \rho_0 + \rho_1(\mathrm{x}) \tag{1}$$

Then we have equation (2) to (3):

$$C^1 = C - C^0,\ e^1 = e - e^0,\ \eta^1 = \eta - \eta^0,\ \rho_1 = \rho - \rho_0 \tag{2}$$

$$U_T = \sqrt{4KTR_1\Delta f_e} \tag{3}$$

The containing inclusions can be simplified into the following integral equation set:

$$f(x,\omega) = f^0(x,\omega) + \int_V \boldsymbol{S}(x-x')(\mathrm{L}^1 F(\mathrm{y}')\rho_1\omega^2 \mathbf{g}(R)\mathrm{T}_1 f(\mathrm{y}')]S(\mathrm{y}')\mathrm{dy}' \tag{4}$$

In view of the following relationship

$$\frac{1}{2\pi}\int_{-\infty}^{\infty} e^{-ik_3x_3'}dx_3' = \delta(k_3) \tag{5}$$

Their matching eigenvectors matrix is shown in the following equation (6):

$$H = [h_1, h_2, ..., h_k] = A^{1/2}E \tag{6}$$

So, we can get:

$$U_{ij} = \frac{H_{ij}}{\sqrt{\sum_{t=1}^{k} H_{it}^2}}, i = 1, ..., n, j = 1, ..., k \tag{7}$$

$$P = I - A^{-1/2}MA^{-1/2} \tag{8}$$

By Bessel function,

$$\frac{1}{\pi}\int_0^{\pi} e^{jmM\pi\sin Y} e^{jnY} dY = J_n(mM\pi)\frac{e^{jn\pi}-1}{2}$$

$$\frac{1}{\pi}\int_0^{\pi} e^{-jmM\pi\sin Y} e^{jnY} dY = J_n(mM\pi)\frac{1-e^{jn\pi}}{2}$$

Then,

$$A_{mn} + jB_{mn} = \frac{E}{j6mn}e^{jm(\pi-\alpha_1)}$$

$$[J_n(mM\pi)\frac{e^{jn\pi}-1}{2} - J_n(mM\pi)\frac{1-e^{jn\pi}}{2}] \tag{9}$$

$$= j\frac{E}{6mn}J_n(mM\pi)e^{jm(\pi-\alpha_1)}[1-e^{jn\pi}]$$

When n=0 or n is the even number, $1-e^{jn\pi}=0$, $A_{mn}+jB_{mn}=0$.

When n is odd number, $1-e^{jn\pi}=2$.

$$A_{mn}+jB_{mn}=j\frac{E}{3m\pi}J_n(mM\pi)[\cos m(\pi-\alpha_1)+j\sin m(\pi-\alpha_1)] \quad (10)$$

$$A_{mn}=-\frac{E}{3m\pi}J_n(mM\pi)\sin m(\pi-\alpha_1) \quad (11)$$

$$B_{mn}=\frac{E}{3m\pi}J_n(mM\pi)\cos m(\pi-\alpha_1) \quad (12)$$

When m=0, $e^{jm(\pi-\alpha_1)}=1$

$$A_{0n}+jB_{0n}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}u_{P1}(X,Y)e^{jnY}dXdY \quad (13)$$

τ is selected as

$$\tau=-\lambda_2 z_2-z_1-F \quad (14)$$

Then we can get:

$$V_2=V_1+\frac{1}{2}z_2{}^T Mz_2 \quad (15)$$

$$\begin{aligned}\dot{V}_2&=\dot{V}_1+\frac{1}{2}z_2{}^T M\dot{z}_2+\frac{1}{2}\dot{z}_2{}^T Mz_2+\frac{1}{2}z_2{}^T\dot{M}z_2\\&=-\lambda_1 z_1{}^T z_1+z_1{}^T z_2+z_2{}^T M(\dot{x}_2-\dot{\alpha}_1)+z_2{}^T Cz_2\\&=-\lambda_1 z_1{}^T z_1+z_1{}^T z_2+z_2{}^T(-Cx_2+Cz_2+\tau\\&\quad-M\dot{\alpha}_1-(G_g+d))\\&=-\lambda_1 z_1{}^T z_1+z_1{}^T z_2+z_2{}^T(f+\tau)-z_2{}^T(G_g+d)\end{aligned} \quad (16)$$

$$\dot{V}_2=-\lambda_1 z_1{}^T z_1-\lambda_2 z_2{}^T z_2+z_2{}^T(f-F)-z_2{}^T(G_g+d) \quad (17)$$

The ideal weight W from (10) and expressed as

$$F=W^T\Phi(\mu) \quad (18)$$

Apparently, the objective function J can be denoted as:

$$\begin{cases}\partial J/\partial k_1=0\\ \partial J/\partial k_2=0\\ \partial J/\partial k_3=0\\ \partial J/\partial k_c=0\end{cases} \quad (19)$$

In general, FPGA is composed by six components, which separately are programmable input and output unit, underlying embedded function unit and embedded specific hard-core. FPGA design flow includes the following sections: design input, integration, adaptation, timing simulation and program download.

4. Results and Discussion

As the DFT and its fast algorithm FFT is a core component of signal processing, the following will through the design of FPGA-based FFT algorithm understand the FPGA applications in digital signal processing, and focus on the design and implementation of butterfly processing unit in the FFT algorithm, a general FFT implementation diagram as shown in figure 3.

In this figure, the computing module is the basis 2/4/8/16 module or their reuse module, ROM table stores N point twiddle factor table. Control module generates all the control signals, read and write addresses of memory 1 and 2, start signal of the operation module, the read address of the factor table, and other signals. Of course, for the operation module which is the basis 16/8 reuse module, the control module needs to generate mode selection signals, for example, for the operation module which is the basis 4/2 reuse module, the signal will decide whether the internal operation module to carry out basis 4 or 2 operation. Memory 1 as the current input symbol corresponds to the N point input buffer, memory 2 as the intermediate result memory is used store the addresses of the results of various channels the operation module calculated, to make them closely co-ordinate, and after some delay to output the operation results and their corresponding indicated signs. The Doppler errors for the T realizations 148 are indistinguishable from the errors shown in Figure 4. The scintillation phase derived from complex signal realization with the proposed algorithm when TYPE=H is shown in the figure 5.

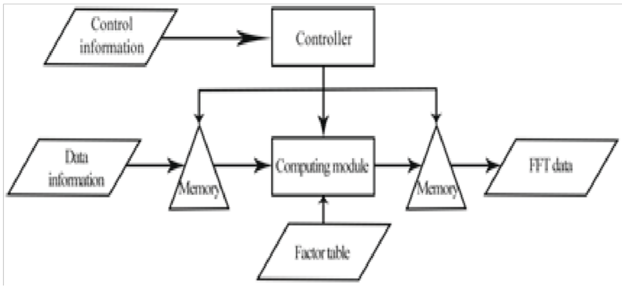

Figure 3. The FFT processing

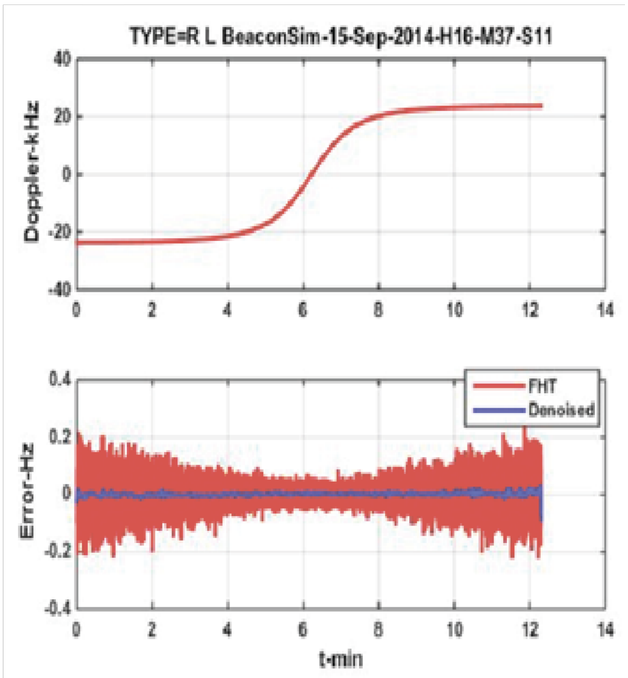

Figure 4. The Doppler errors for the T realizations 148

External input is N point data flow and the start signal, on the one hand, the external data is stored in the memory 1, at the same time through the control by the control module the preceding N point data in the memory 1 and the factors in the ROM table, as well as the related control signals are sent to the operation core module for all Pass operations, and each Pass output is stored in the memory 2 and when the next start arriving the results will be exported. The implementation of figure 3, except for computing module, the key is the cooperation of each Pass data factor read and write address with the control signals.

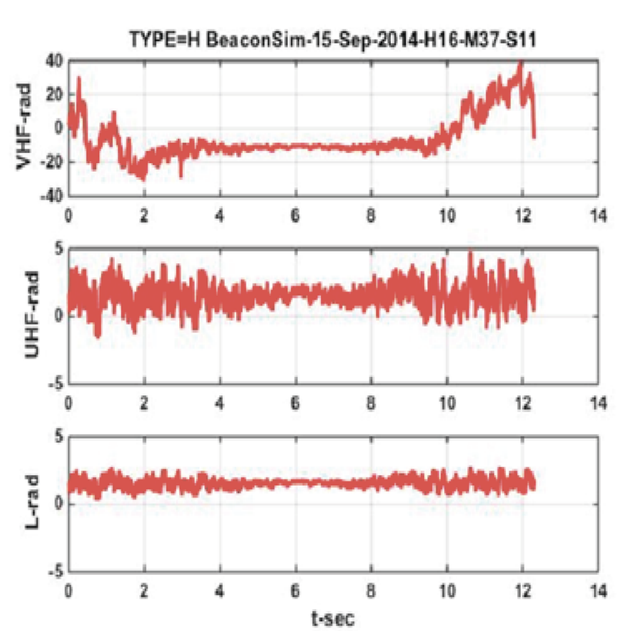

Figure 5. The scintillation phase derived from complex signal realization with the proposed algorithm when TYPE=H

5. Conclusions

In this paper, the author studies about the digital signal processing algorithms of high speed digital circuit in physical layer. At present, the digital signal processing has applied extensively in many subjects such as communications, radar, sonar, speech and image processing etc. Digital signal processing is to use a computer or special processing equipment to collect, transform, filter, valuate, enhance, compress and identify the signal, to obtain the signal form met the needs. The essential of the digital signal processing technology is to convert the analog signal or some signals in real life into digital signals and carry out corresponding processing for the converted digital signals. In order to solve the problem of performance degradation which arises from sequence truncation in many digital signal processing occasions, this paper prompts an algorithm for the digital signal processing algorithms of high speed digital circuit in physical layer. The experiment result shows that the performance can be improved by using this algorithm.

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