Synchronous Measuring System on Time Intervals of Multiplex Pulse-Signals Based on FPGA & ARM 7

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Abstract

In this paper, we propose a design scheme of synchronous measurement system on time intervals of multiplex pulse-signals based on FPGA and ARM7, including acquisition and measurement circuit, data analysis circuit and other auxiliary circuit. The acquisition and measurement circuit is designed to synchronously measure respective time of 20 random pulse-signals traveling from the edge to the trigger signal, and to easily achieve parallel expansion of more channels. The hardware circuit design, software design and the simulation result are introduced, from which we can guarantee the time accuracy of less than 5us. The FPGA chip applies the EP1C12Q240C8N of Cyclone Series and the ARM7 control chip applies the LPC2214, using respectively the Verilog hardware description language and C programming language to design related software.

Key words: FPGA, ARM7, MULTIPLEX PULSE, TIME INTERVAL

1. Introduction

With the rapid development of computer technology and mobile communication technology, signal acquisition is developing towards the direction of multi-channel, high speed and intelligence. In signal processing area, system of acquisition and processing on multiplex pulse signals is widely used in the field of military and space such as radar system, missile equipment, communication system, and so on [1]. In order to analyze the system more quickly and comprehensively, the related signals are usually measured in the process of measuring the main signal.

The traditional pulse signal measuring system has a lot of problems, such as hard to synchronize, limited channels, poor applicability and so on, whose limitation in dealing with the position of high speed and high performance is becoming more and more obvious.

FPGA is suitable for measuring multiplex pulse signals because of its high frequency of internal clock,

short delay of logic gates, abundant resources of I/O interface [2]. ARM7, as a kind of powerful, flexible and variable CPU, is suitable for designing the measuring system with the C Programming Language and the embedded Linux operating system, from which its performance can be exerted to the best [3]. This paper puts forward a design scheme based on ARM and FPGA to measure multiplex pulse signals, including collection unit, calculation unit, storage unit, display unit and so on.

2. Working principle of the system

2.1. Composition of the system

The whole system is composed of signal acquisition part and data-processing part. The signal acquisition part is designed to collect multiplex pulse signals, calculate time interval and correct the error and data-processing part is used to receive data, get current time information, save data into storage device, and display data in LCD dynamically. The system begins with the jump of a trigger signal to calculate the time intervals from every rising edge (or falling edge) to the jump of a trigger signal in each signal channel. The sequence diagram of system function is shown in Figure 1.

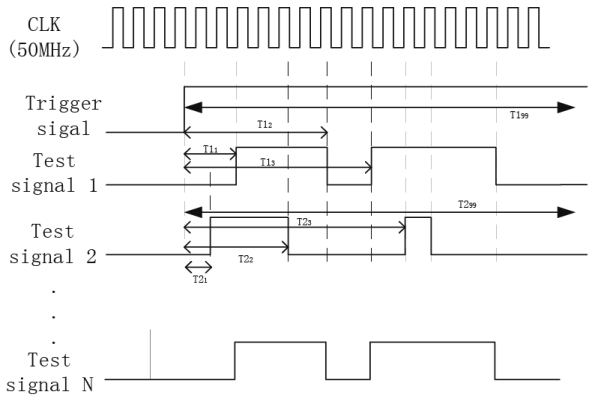

Figure 1. Sequence diagram of system function

2.2. Error analysis

The required accuracy of this system is less than 5us, determined mainly by the clock accuracy of FPGA, the sampling frequency and the delay precision of the peripheral circuit. As the sampling frequency of the system, external clock of FPGA uses a 50 Mhz-oscillator to ensure the time resolution of 20ns.

When the jump of the trigger signal happened, the delay time of ΔT1 appeared because four-level of registers as a buffer were used in order to eliminate the metastable state and filter the glitches. After the jump, the counter started to work at the rising edge of the next clock cycle to bring delay time of ΔT2.So, during the period from the jump of the trigger signal to the start of the counter, a relative stable error was caused by the delay of the chip internal logic circuit:

$$T_1 = \Delta T_1 + \Delta T_2 \quad (1)$$

The above edge detection method was also used in measuring each signal channel. So, delay time of ΔT3 and ΔT4 appeared, similar to ΔT1 and ΔT2 respectively. When system detects the jump of measured signal in each time, latching counter-value and edge detection took one clock cycle and four clock cycles respectively. However, the counter was still working during these clock cycles. So, the delay time for the N time of jump should be:

$$T_N = T_1 + \Delta T_3 + \Delta T_4 = \Delta T_1 + \Delta T_2 + (N-1)(\Delta T_3 + \Delta T_4) \quad (2)$$

$$T_N = 4T_{CLK} + T_{CLK} + (N-1)(4T_{CLK} + T_{CLK}) = 5NT_{CLK} \quad (3)$$

The above delay time belonged to the incremental error. The error would be corrected in software design, in which latching counter-value was subtracted by 5*current jump times in each time.

3. Hardware design

The hardware design is composed of signal acquisition part and data-processing part, in which the acquisition and measurement circuit, data analysis circuit, calendar circuit, memory circuit, LCD display circuit and the communication circuit will be given in detail. The hardware block diagram is shown in Figure 2.

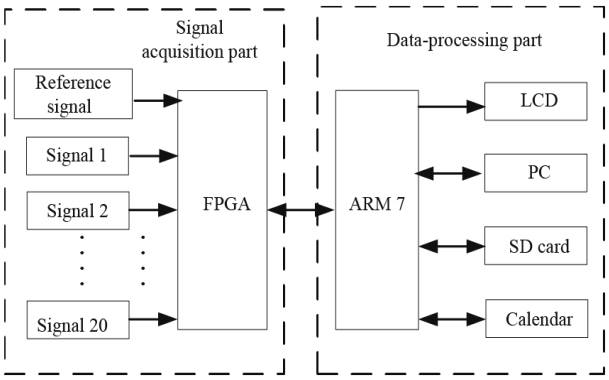

Figure 2. Hardware design diagram

3.1. Design of CPU's minimum system

The acquisition and measurement module applies the high-speed FPGA EP1C12Q240C8N of Cyclone Series, whose system frequency can exceed 200MHz after doubling the internal PLL frequency. As the mainstream products, it is a medium size FPGA, using 0.13um process, 1.5V power supply for core, QFP240 package and more than 20000 logic units, which is a low cost FPGA chip. [4] The data analysis module applies the ARM7 chip LPC2214. It has 128 bits wide memory interface and unique acceleration structure, so that the 32 bits code can run at maximum clock rate. The maximum operating frequency is up to 70MHz. [5]

The circuit of the minimum system includes a power supply circuit, the reset circuit and the oscilla-

tor circuit. The power supply circuit provides 3 kinds of different voltages: 5V, 3.3V and 1.8V respectively. The core of which is the communication interface circuit between LPC2214 and FPGA [6].

3.2. Design of interface circuit between FPGA and ARM

There are two communication interfaces between FPGA and ARM: parallel mode and serial mode. The former one runs in high speed, which requires more communication pins of ARM yet. The latter one requires only two communication pins of ARM, which runs in low speed yet. UART, one of serial communication mode, was applied in the design, because less pins of LPC2214 were left to connect FPGA and it was not critical for communication's working speed. [7]

The 136th pin of FPGA is the TXD of UART and the 135th pin is the RXD of UART, which were connected to P0.1 and P0.0 of LPC2214 respectively.

3.3. Design of input circuit

Both trigger signal and test signals are off-on signals, which is shown in Figure 3. When acquisition and measurement module receives the trigger signal, the counters for each channel begin to work immediately and monitor the jumping state of each signal at the same time. Both the rising edge and the falling edge can start the counter. The program used edge detection to realize the logical operation to the external trigger signal.

In order to prevent the measuring system from external disturbance, 6N137, a kind of optical isolator, was designed to develop the total performance [8], which was shown in Figure 4. The external signal 01_IN was connected to the 2nd pin of 6N137, which was transferred into 01_OUT signal to connected FPGA to be measured.

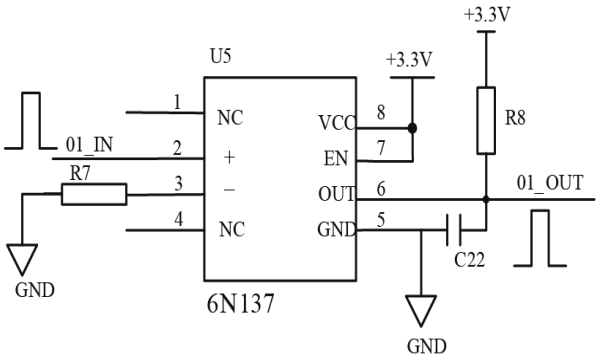

Figure 3. Input circuit

3.4. Design of display circuit

This circuit mainly consists of 240*128 LCD and the PC communication, achieving the man-machine interactive function. Instrument applies the CA240128E LCD to display the measured channel, time interval, interval number and other information in real time.

The C++ programming language was applied to design the software of PC on the VS development platform. Related information of the measured signal can be displayed in the software. PL2303 was used to achieve USB to serial. The principle is shown in Figure 4.

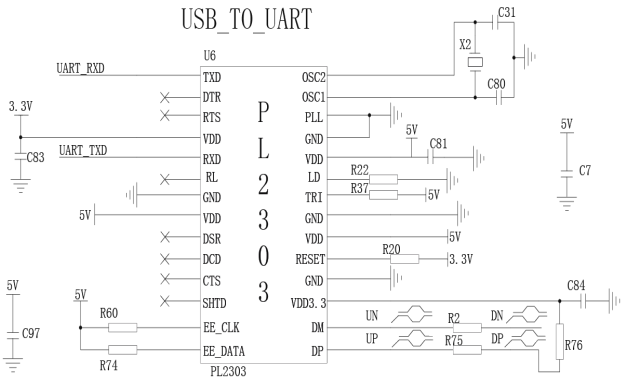

Figure 4. Display circuit

3.5. Design of storage circuit

This circuit is implemented by Class4 SDHC, which is used to store the parameters of the signal channel and a large amount of time interval information.

Class4 SDHC, a kind of SD card produced which by Kingston capacity of 32G, is based on the SPI bus. Data can be stored for a long time without lost, which is convenient to inquire. The principle is shown in Figure 5.

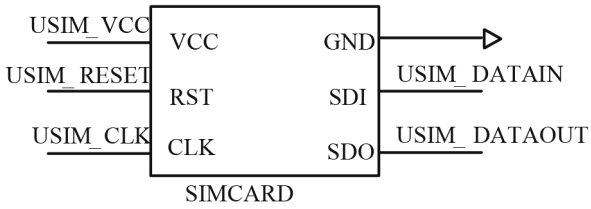

Figure 5. Storage circuit

3.6. Design of calendar circuit

PCF8563, a multi-function clock/calendar chip based on I2C bus, was designed as the calendar circuit.

When the ARM tries to store the data, the time information provided by the clock module is stored in the SD card as a time stamp at the same time, which is convenient for the latter query. When the system is not working, it can also provide time information for the upper monitor and LCD display. In order to ensure its continuous operation, a 3V button battery is used as its power supply and a large capacitor connects to the power pin, preparing for working while battery exchanges [9]. The principle is shown in Figure 6.

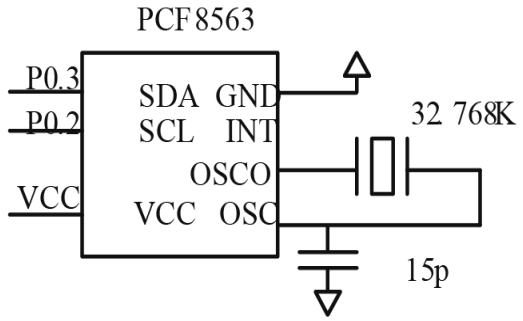

Figure 6. Calendar circuit

4. Software design

4.1. Design of acquisition and measurement function

The acquisition and measurement function is completed by FPGA, in which Verilog hardware description language is used to program from the development platform-QuartusII. There are edge detection, digital filter, FIFO cache, counter, timing constraint and other technology in the design [4], of which top level schematic document is shown in Figure 7.

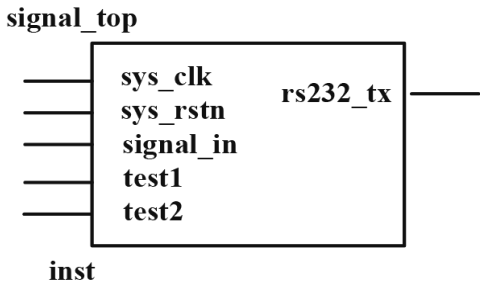

Figure 7. Acquisition and measurement function

In the top-module, symbol of sys_clk is system clock and the external oscillator's frequency is 50MHz. Symbol of sys_rstn is system reset, multiplexed by each module, resets asynchronously while releases synchronously. Symbol of signal_in is the input port of trigger signal. Both of the rising edge or the falling edge can start the counter. Symbol of test1 and test2 are the first two of 20 channels. Symbol of rs232_tx is the send port of the serial bus, which communicates with ARM7.

4.2. Design of analysis and storage function

Except acquisition and measurement function, all the other functions are designed by ARM7 processor. C programming language is used to program, which is compiled and debug by ADS development environment. The main function is shown in Figure 9.

5. Experiment results and analysis

The high precision signal-generator is used to generate 16 jump signals as expected, whose interval time are 20us, 40us, 50us, 60us, 100us, 140us, 240us, 340us, 390us, 440us,580us, 720us, 800us, 880us, 940us, 1000us respectively. From measuring these signals, practicability and precision of the system is justified. The results are shown in Table 1.

Table 1. The values of time in the mill drum first section

Original time (us)	Measured parameters		
	Real pulses	Measure time (us)	Error (us)
20	1001	20.02	0.02
40	2001	40.02	0.02
50	2501	50.02	0.02
60	3001	60.02	0.02
100	5001	100.02	0.02
140	7001	140.02	0.02
240	12000	240.02	0.02
340	17000	340	0
390	19500	390	0
440	22000	440	0
580	29000	580	0
720	36000	720	0
800	40000	800	0
880	44000	880	0
940	47000	940	0
1000	50000	1000	0

From the above table, measure time is almost equal to real time. The biggest error is 0.02us, which is very small. Such precision can meet requirement.

6. Conclusions

This thesis puts forward a design method and implementation scheme based on FPGA and ARM7 of synchronous measurement on the time intervals of the multiplex pulse signals. The two control chips, functioning adequately, ensure not only the correctness and fast of data acquisition, but also the stability of the system. From experiment results, the biggest error is 0.02us when the frequently used signals are measured. The measuring precision can meet requirements.

Acknowledgements

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