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Design and implementation of material position detection system based on FPGA

Lei Zheng*

Electrical and Electronic Experiment Center of Southeast University, Nanjing, 211189,China

Renjie Hu

School of Electrical Engineering, Southeast University, Nanjing 210096, China

Yang Zhao

Department of Electronic and Information Technology,Jiangmen Polytechnic,Jiangmen 529090,Guangdong,China

Jinming Bao

College of Automation, Southeast University, Nanjing 210096, China
*Corresponding author,
Email: Zhenglei0217@163.com

Abstract
According to the actual demand of heavy hammer type material position detection, a FPGA-based intelligent control system is proposed in this paper. Started from the design principle of the whole system, hardware development is introduced in detail. Software control module of FPGA and communication bus module are achieved by Verilog HDL, the D/A conversion and transmission of the measurement data is implemented by AD5422 chip. Improvement ideas are also raised to solve exceptions like twisted rope or buried hammer. Thereby intelligent functions such as material position automatic detection, fault alarm and repair, interactive interface and remote data transmission are also implemented in the system. After a series of field tests, it is proved that this system is stable running, reliable performance and low cost.
Key words:MATERIAL POSITION DETECTION, HEAVY HAMMER, FPGA, TRANSMISSION, DESIGN

1. Introduction

The research and development of solid material position detection has important significance for grain storage[1], coal mine and chemical industry. The detection method mainly contains capacitance detection, ray detection, ultrasonic detection, radar detection and hammer detection[2,3,4], of which the first four detection methods are costly, seriously susceptible by environment and with a complex installation process[5]. But the detection method based on heavy hammer has simple structure, high precision and strong anti-interference capability, therefor it is widely used in industry field.

A heavy hammer detection system based on FPGA(Field Programmable Gate Array) [6]technology is introduced in this paper. In this design, the hardware and software structure of detection system are both improved. The development process of FPGA is introduced in detail, also are the solutions to solve exceptions like twisted rope, buried hammer, electromagnetic interference and wrong position. In a word, this solid material position detection system has accurate measurement and intelligent design.

2. The system structure and detection principle

Heavy hammer position detection system is an electromechanical integration system based on intelligent control technology. The whole system consists of mechanical implementing agencies, control subsystem and display subsystem.

Mechanical implementing agencies include disk, three-phase asynchronous motor, speed reducer, encoder, pulley, steel cable and heavy hammer. Control and display subsystem is made up of keyboard input module, display module, motor drive module and code disc counting module, at the end the measurement result is exported as 4-20mA current signal. The control and display subsystem is based on FPGA, it carries out the intelligence and distributed control of material position detection.

The whole detection system timely drives heavy hammer to rise and fall by controlling motor to rotate positively and negatively. When the periodic sense command is sent by the controller, the motor rotates in forward direction, it makes the rope down and drives the hammer fall down from the warehouse roof, at the same time the controller takes count of the encoder signal, calculates the drop height. When the hammer reaches the solid material level surface, the heavy hammer is lift up with weightlessness and the slack of wire rope is caught by tension sensor which makes the counter to stop. The difference between the value observed in the last two samples shows the height from the warehouse top to solid material level surface. Then comes the reset process, the command is sent, the motor rotates inversely, hammer is lift up to the roof. Till now, one complete detection process is finished, meanwhile the measurement result is displayed in local screen and also sent to remote monitor as 4-20mA current. In a word, this detection mechanism is simply, reliable and efficient.

3. Hardware Design and Implementation

3.1. The control module-FPGA

The control core of this detection system is made of FPGA. Unlike the traditional system based on PLC or Single Chip Microcomputer, the hardware design based on FPGA has many advantages, such as low cost, high density and reconfiguration. The stability of system can be enhanced by using hardware redundancy, time redundancy, error-correcting codes and detection technology[7]. In order to increase the competitiveness of our product, we need to develop our special ASIC in a short time, special layout tools are used to reprogram the internal standard cell array. Since FPGA is a pure hardware controller, it can achieve high performance by using parallel processing without taking up system resource. Hence the system can work stable over a long period of time even in a complicated environment[8].

Spartan-6 FPGA adopts efficient, dual-register six-input LUT logic structure and the industry's leading Virtex architecture, including 18Kb Block RAM, DSP48A1 Slice, enhanced mixed mode clock management features, system-level power management features, auto-detect configuration option. Each

DSP48A1 slice contains a fast 18 x 18 multiplier and a 48-bit accumulator capable of operating at the highest rate of 390MHz, it provides pipelining and cascading capability to enable cross-platform compatibility and to improve system performance. These blocks make for greater system-level integration than ever before.

3.2. Hardware Design and Implementation

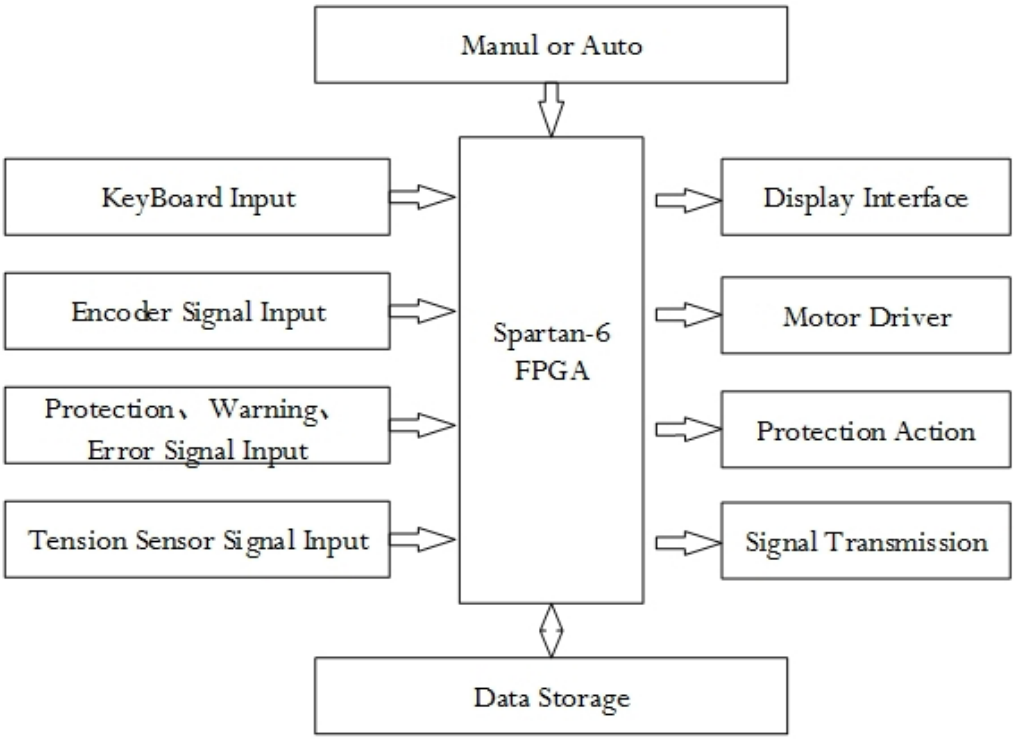

Figure 1. Hardware block diagram of system

The hardware framework of the material position detection system based on FPGA is shown in Figure.1. It is comprised of a FPGA controller, on-site keyboard, data display module, over-range alarm and protection, motor drive, data conversion and transmission, height measurement module and so on. Figure.1 also shows the input and output relationship of data signals and control signals. System parameters are setup by users through keyboard, and stored in EEPROM. After measurement, the results are transformed to a 4~20mA current by signal transform module, and sent to remote monitor.

The Xilinx Corporation's Spartan-6 FPGA chip XC6SLX45-3CSG484 which is low cost and low power, is selected as core controller. Its peripheral circuit and power supply circuit are designed according to the system demand. Through the adoption of IO interface scanning, the keys module actualizes measurement-mode selection and manual/auto mode selection function. Digital acquisition and input module is used to gather limit, protection and alarm input signals. Digital level signal is used to show the status of tension sensor, when the hammer reaches the position level of solid material, high level signal is produced by tension sensor, otherwise it's low. Other output signals, such as protection signal, alarm signal and motor driver signal are also digital signals, as FPGA is good at parallel digital signal processing.

3.3. Data display module

Nixie tube is used in digital display module as it's simple and stable. The MAXIM Corporation's MAX7219 chip is driven by FPGA to display measurement mode and results dynamically. MAX7912 is a compact, serial input/out-put common-cathode display driver. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. It use SPI bus to exchange data with FPGA.

3.4. Data storage and transmission

The Atmel Corporation's 2k serial CMOS E2PROM chip AT24C02 is used to store material position data in this system. It use IIC bus to transfer data, the interface ports are SCL, SDA. A high-to-low transition of SDA with SCL in high status is a start condition. A low-to-high transition of SDA with SCL in high status is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode.

The ADI Corporation's chip AD5422 is used in data transmission module. The AD5422 is a low-cost, precision, fully integrated 16-bit converter offering

a programmable current source. The output current range is programmable to 4~20 mA, 0~20mA or 0~24mA. When the output current is configured as 4~20 mA, the current value is:

$$I_{OUT} = \left[\frac{16mA}{2^N}\right] * D + 4mA$$

In this formula, D represents the measurement result sent to DAC by FPGA, N is bit resolution of DAC. The related circuit of AD5422 is shown in Figure.2, 3-wire serial interface, SDIN, SCLK and LATCH are used to communicate with FPGA, using SPI protocol. It can work at highest 30MHz, and meet the output demands by configuring control register.

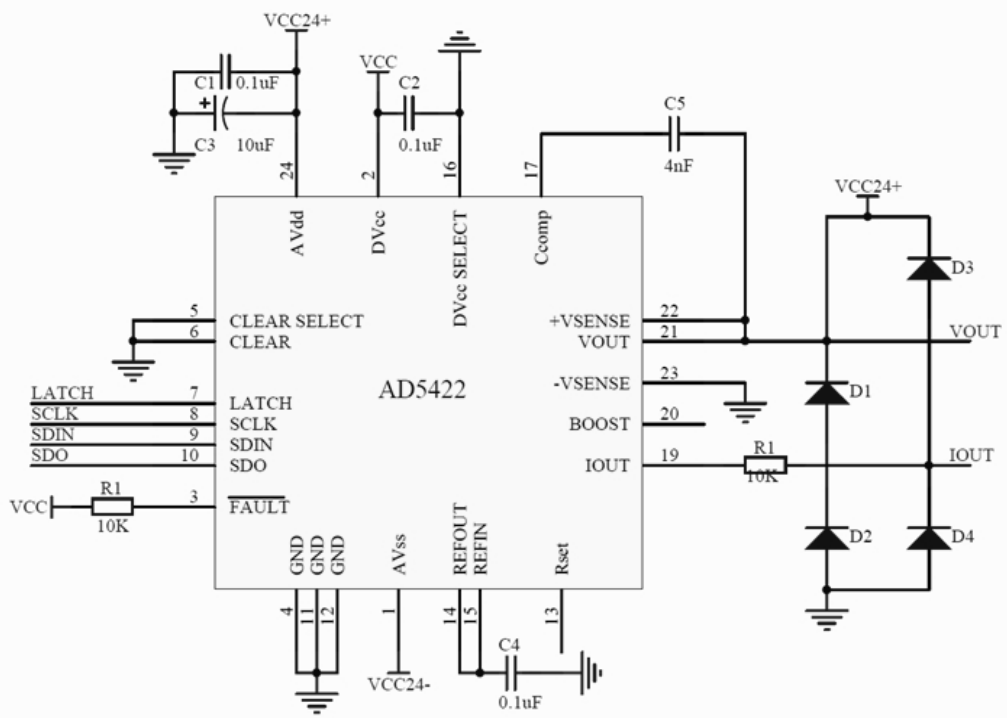

Figure 2. Circuit diagram of AD5422

Timing diagram is shown in Figure.3, the write mode of AD5422 takes about 24 clock cycles, 24 bits are written to the input shift register, which include 8 address bits and 16 data bits. Data from the SDIN port is imported on the rising edge of SCLK, and is latched on the rising edge of LATCH.

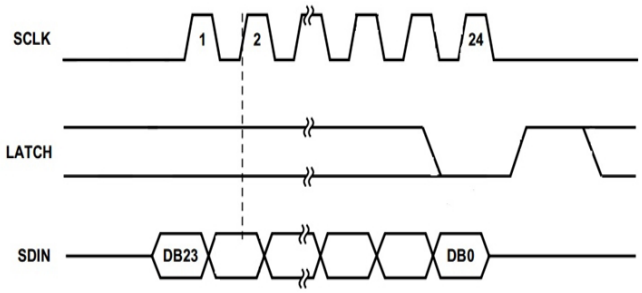

Figure 3. Timing diagram of SPI

4. Software development

ISE(Integrated Software Environment) is used to do the software development in this system, which is developed by Xilinx corporation. Design process includes design entry, Synthesis, Implementation, Verification and Download.

The system software is designed with Verilog HDL, using bottom-up design idea. Logic diagram is used on top level as shown in Figure.4. After system power-on, the default system parameter is read from EEPROM firstly. Then according to different mode selected by keyboard, the system parameter will be setup by pushing setup key, if the setup key isn't pushed after 5 seconds, measurement mode will be selected. In measurement mode, three processes are handled in the same time, which are data measurement,data display and data transmission module. Measurement results are delivered to MAX7219 in time for display. Results are also converted to 4-20mA current by AD5422 and sent to monitor. In measurement process, manual mode or auto mode can be selected. In manual mode, if measurement key is pressed, hammer falls down to the material level surface. If the return key is pressed, hammer is lifted up to ceiling. In auto mode, hammer is lifted up and down peciodirally according to the preset measurement period.

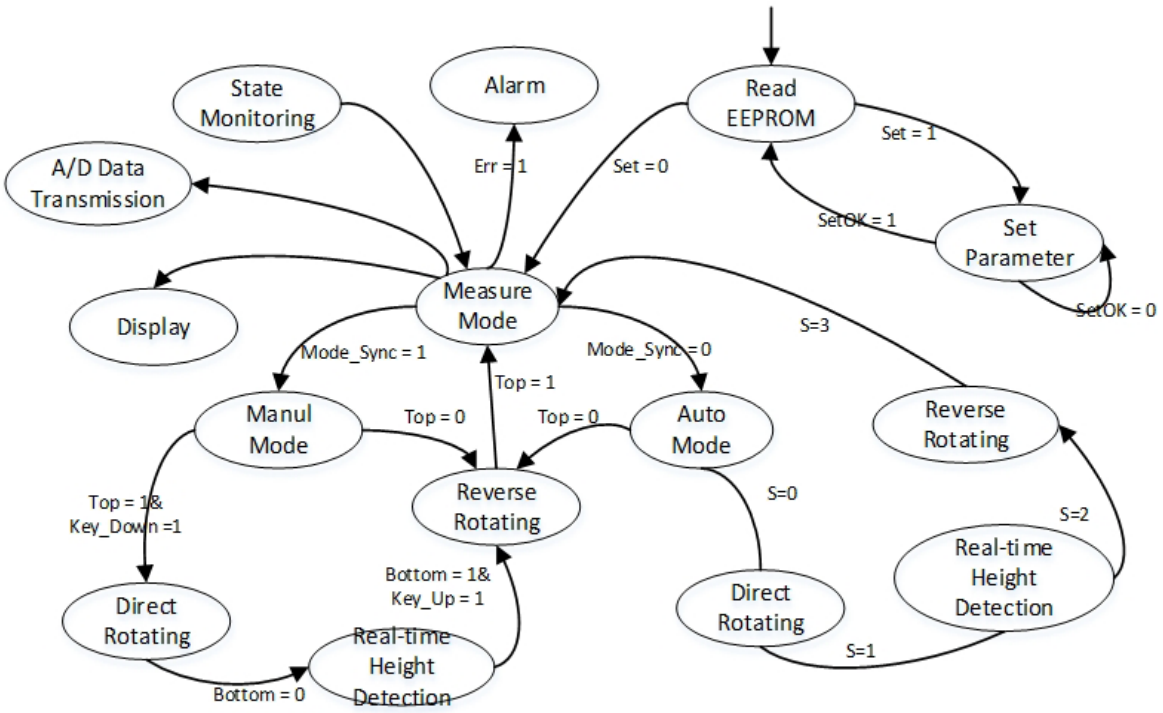

Figure 4. Logic diagram of software design

SPI and IIC bus are used in this system for parallel operations between FPGA and peripherals, such as AT24C02, Max7219, AD5422. Time state machine and sequential operation are used in software system to implement timing Sequence Simulation and data processing.

4.1. IIC bus implementation

IIC bus is used to store and setup measurement cycle and range in AT24C02. Full duplex transmission of data is implemented using a serial clock line (SCL) and a serial data line (SDA). To meet the exact time sequence, serial clock line (SCL) is used to send clock pluses, while serial data line (SDA) is used to transmit data.

Data transmission sequence is shown in Figure.5. After the start bit S, a 7-bit slave address is sent. Then followed a data direction bit (R/W), 0 means writing data, while 1 means reading data. At last, a stop bit (P) sent by master machine stops the data transmission.

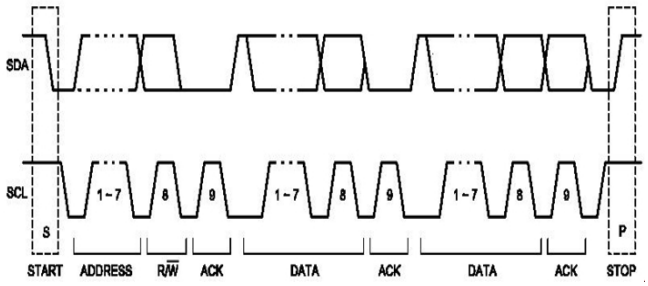

Figure 5. Data transmission sequence

Finite state machine is used to implement IIC time sequence with FPGA. The state machine can be divided into 5 states, IDLE, START, SEND, RECEIVE and STOP. And it can also be subdivided into 12 states, using one-hot state coding method.

parameter IDLE = 12'b000000000001;
parameter START1 = 12'b000000000010;
……
parameter STOP = 12'b100000000000;

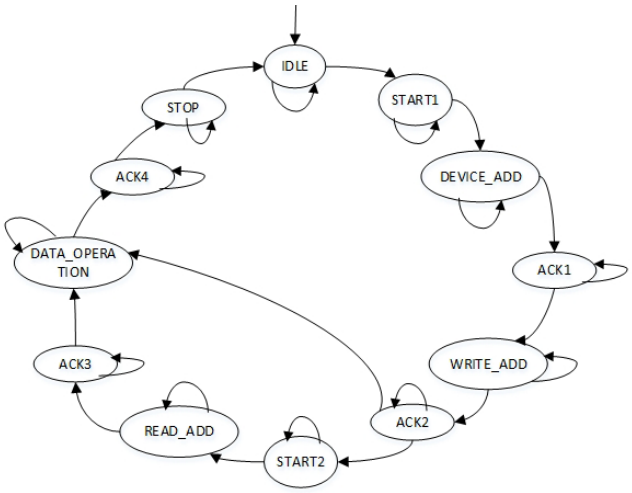

Figure 6. State transition diagram

State transition diagram is shown in Figure.6, which implements reading and writing of system parameters.

4.2. SPI bus implementation

SPI bus is used to transit data between Max7219,

AD5422 and FPGA. Time sequence of AD5422 refers to Figure.3. According to the principle of system synchronization, SCLK and LATCH signal are sent out on time tick CLOCK_50. At the same time, 24-bit data is loaded into AD chip, which includes 8-bit address and 16-bit data. After then, measurement result is converted to 4-20mA current. Part of code is as follows.

```
always@(posedge CLOCK_50)
 begin
      ……
case(da_ref_cnt)
2,6,10,14,18,22,26,30,34,38,42,46,50,54,58,62,66,70,74,78,82,86,90,94:
AD5422_SCLK <= 1;
0,4,8,12,16,20,24,28,32,36,40,44,48,52,56,60,64,68,72,76,80,84,88,92,96:
AD5422_SCLK <= 0;
default : ;
……
case(da_ref_cnt)
  0,100: AD5422_LATCH <= 1;
  98: AD5422_LATCH <= 0;
default : ;
……
case(da_ref_cnt)
1,2: AD5422_SDIN<=address[7];
  ……
29,30:AD5422_SDIN<=address[0];
33,34:AD5422_SDIN<=datah[7];
  ……
61,62: AD5422_SDIN<=datah[0];
65,66: AD5422_SDIN<=datal[7];
……
93,94: AD5422_SDIN<=datal[0];
default : ;
```

5. System Reliability Design

The working surrounding of hammer material level meter is complicated that there are a great deal of factors in influence of the normal operation and machine life[9][10], such as electromagnetic interference, dust, moisture and other harmful substances. Therefor, stability is the key point of system design, this chapter introduces several improvement plans to enhance the stability of the system.

5.1. Hardware anti-interference design

Reasonable isolation from electromagnetic interference on site is taken to reduce external interference. State sensors are placed in some key positions such as tension sensor, warehouse roof and motor, in order to monitor system status, moreover, to adjust the working process according to system state. Meanwhile, due to the small size of FPGA, the controller is put in a sealed container to avoid moisture, dust violations. More suggestions are also given in this chapter according to the following three conditions:

The problem of rope-handing is the main error generation source in system. Take climbing rope for example, assume that the original rope groove diameter is D, and the rope diameter is d, then the errorδ is:

$$\delta = 2\pi * (d + D) - 2\pi D = 2\pi d$$

In order to avoid such errors in the system, rope drum with deep groove is adopted to make rope warp around the wheel in accordance with the direction of thread. The design can avoid twisting rope and climbing rope in motor reversing process, which also improve the measurement accuracy of the system.

During the measurement process, once the hammer gets buried under material powder, motor will be packing up, the fault light will be on and alarm signal will be sent to host computer to ensure the safety of the system.

5.2. Software anti-interference design

D flip-flop is adopted in the hardware design in order to eliminate interference signals. Synchronous sequential logic design method is used to make the system work in a single clock domain and reduce the risk caused by race and hazard. The state transition condition of state machine in the system software (Figure. 4, Figure.6) is implemented by One-hot coding, which can also enhance the system stability.

6. Results and Analysis

The system integrates all the control circuits in one single PCB board, it has advantages such as small in size, dust-proof, fire-resistant, corrosion-resistant, explosion-proof and so on. Therefore, it can be widely used in all kinds of material position measurement environment, such as building material, metallurgy, mining, chemical, electric power industries etc. The system also has several control modes(manual, automatic, jog, hand and remote control). Exceptions like twisted rope, buried hammer and other abnormal phenomenon during measurement process can be effectively prevented. The intelligent alarm function and safeguard mode of this system can also ensure the system stability.

After more than 1000 times experimental results

with at least 129 hours continuous working time in a signal experiment, the system can achieve the technical target as follows:

I. Measurement Range: 0-35m
II. Measurement Accuracy:
Length error: <± 0.5cm/m
Percentage error: <± 0.5%
III. Detection Speed: 8m/min
IV. Data Output: DC 4-20mA current signal
V. Digital Display: 4 digit LED display
VI. System Host Protection level: IP65
Several experimental results are shown in Table.1:

Table 1. The experimental results

Experiment times	Standard value/m	Measurement result /m	Error
1	0.755	0.753	0.2%
2	13.467	13.466	0.01%
3	25.582	25.582	0
4	34.812	34.814	0.006%

7. Conclusions

The material position detection system based on hammer is widely used in industry. Apart from other systems based on MCUs or PLCs, this system uses FPGA hardware design technology, which has simple hardware circuit and more perfect software design which improves the system stability. The test results show the system has high reliability, good applicability, low cost and intelligent detection functions. It has very good practical value.

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